64000

HP64000 Logic Development System

Model 64602A Timing Acquisition Board

HEWLETT PACKARD

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CW&A 2/81

HEWLETT-PACKARD

SERVICE MANUAL

MODEL 64602A

TIMING ACQUISITION BOARD

REPAIR NUMBERS

This Manual applies directly to Models
with Repair Numbers prefixed 2148A.

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LOGIC SYSTEMS DIVISION
COLORADO SPRINGS, COLORADO, U.S.A.

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Manual Part Number: 64602-90902
Microfiche Part Number: 64602-90802

PRINTED: OCTOBER 1982
CHANGED: NOVEMBER 1982

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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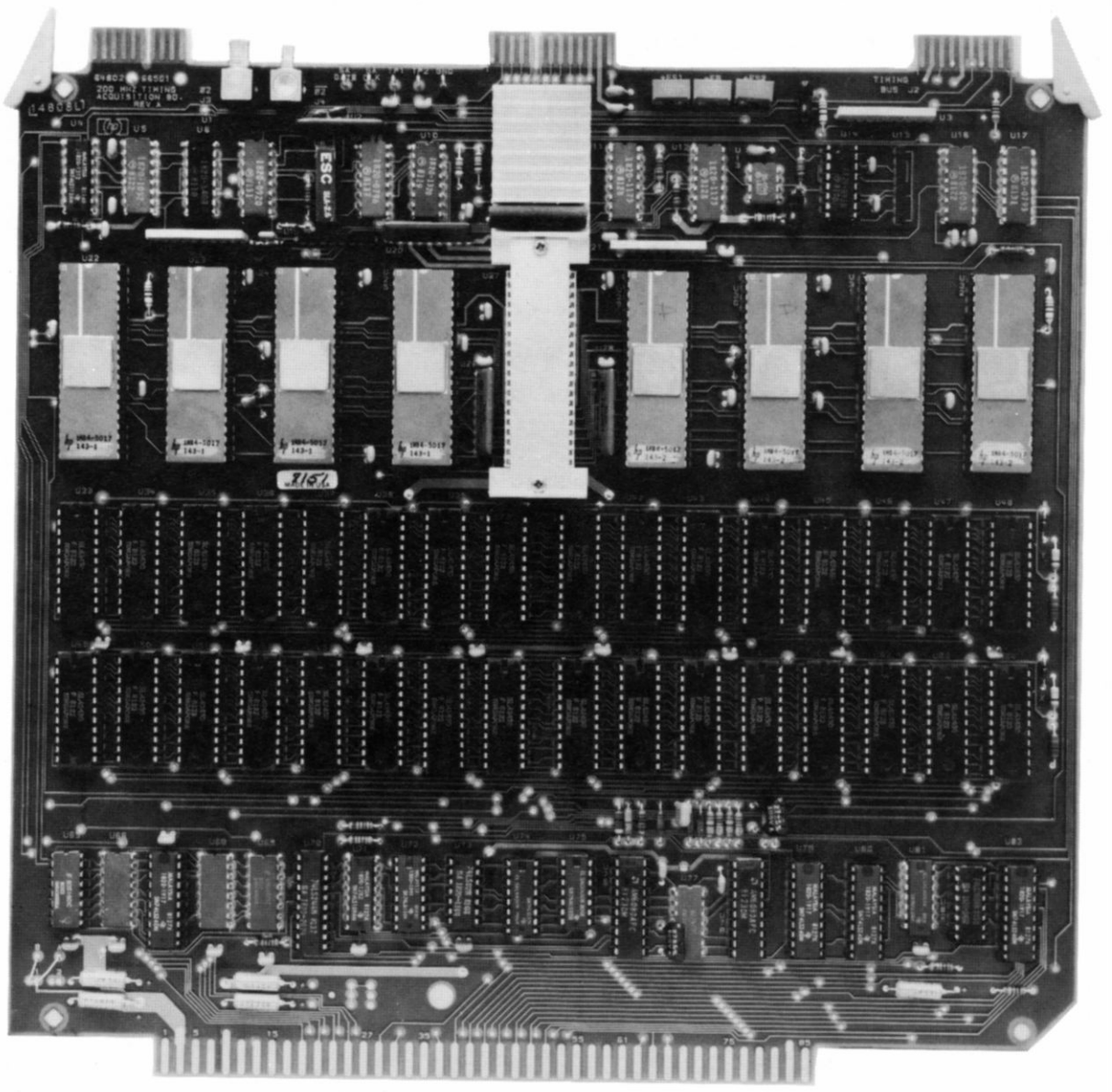

Figure 1-1. Model 64602A Timing Acquisition Board

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Service Manual contains information required to install, test and service the Hewlett-Packard Model 64602A Timing Analysis Acquisition Board. Operating instructions are provided in a separate Operating Manual supplied with the instrument.

1-3. Shown on the title page is a microfiche part number. This number can be used to order 4X6-inch microfilm transparencies of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

1-4. INSTRUMENTS COVERED BY THIS MANUAL.

1-5. Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form: 0000A0000. It is in two parts; the first four digits and the letter are the repair prefix, and the last five are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-6. An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual for the newer instrument.

1-7. In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-8. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Office.

1-9. DESCRIPTION.

1-10. The Timing Analyzer is used to monitor information flow in the time domain. The information may be a software program, the actions of a hardware state machine, or random logic signals.

1-11. The Timing Analyzer consists of one Model 64601A Timing Control Board, and from one to two Timing Data Acquisition Boards.

1-12. Up to two Acquisition Boards may be combined to form a Timing Analyzer with as many as 16 channels.

1-13. Logic Analyzers within one Mainframe may be connected together using the Inter Module Bus (IMB). One possible use of the IMB is to allow a State Analyzer to trigger a Timing Analyzer.

1-14. SPECIFICATIONS.

1-15. Instrument specifications are listed in Table 1-1. These specifications are the performance standards or limits against which the instrument is tested.

Table 1-1. Specifications.

Includes Models 64601A Control Board, 64602A 8-Channel Acquisition, and 64604A 8-Channel Timing Probes.

Sample rates
- Wide Sample Mode: variable from 2Hz to 200MHz.
- Glitch mode: variable from 2Hz to 100MHz.
- Dual Threshold: same as Wide Sample Mode.
- Fast Sample: 400MHz.

Memory length:
- Wide Sample, Glitch, & Dual Threshold Modes: 4060 samples.
- Fast Sample Mode.....: 8140 samples.

Memory width (8 channel system)
- Wide Sample.....: 8 channels.
- Dual Threshold, Glitch, and 400MHz modes: 4 channels.

Memory width (16 channel system--two acquisition boards)
- Double the width for a single, 8-channel system.

Resolution:
- Total skew from probe tip:
  - Within pod: +/- 1.5ns.
  - Pod to pod: +/- 3.0ns.
    - Conditions: Input signal: VH = -1.0V, VL = -1.6V, VTH at -1.3V
      Input slew rate > .25 V/ns
- Sample rate accuracy: typically +/- .002%

Probe characteristics
- Input Z: 100K ohms +/- 2%, shunted by <6pf.
- Drive requirements:
  - Minimum input amplitude: 600mV P/P.
  - Minimum input overdrive: 200mV or 25% of input amplitude, whichever is greater.
  - Minimum input pulse width: 3.0ns at threshold.
- Dynamic range: +/- 10V.
- Maximum input: +/- 40V.
- Threshold accuracy: +/- 50mV or +/- 2% whichever is greater.
- Hysteresis: Typically 50mV.

Glitch Mode
- Maximum sample rate: 100MHz.
- Minimum width: 3.0ns at threshold.
- Maximum width: sample period less 4.0ns.

Specifications (continued)

Triggering

Time duration accuracy: +/- (20% + 2ns).
Minimum width for narrower-than trigger: 6ns typical.
Minimum width for transition trigger: 6ns typical.
Displayed position accuracy: +/- 4 samples in Wide Sample, Dual Threshold, and Glitch Modes.
: +/- 8 samples in Fast Sample Mode.
Delay from input to external BNC drive: Typically 60ns.
Delay from input to internal IMB drive: Typically 55ns.
Dead time for post-qualify measurement reset.
Typically 50ns + the time required to fill the memory with the selected amount of pre-trigger information.
Reset time for duration trigger: To meet the duration specifications, the trigger duty cycle must be no greater than 40%.

BNC Drive

Output signal swing in transition trigger mode:
Amplitude: 2.0V typical.
Width at 50%: 10ns typical.
Output signal swing in width greater-than trigger mode:
Amplitude: 2.5V typical.
Width: Input trigger width minus the selected duration.
Output signal swing in width less-than trigger mode:
Amplitude: same as in transition trigger mode.
Width: same as in transition trigger mode.

Position: occurs when trigger pattern disappears, before the selected duration times out.

IMB Functions (interconnection with other modules):

Master Enable (LE/ME)-------: drive, receive (Execute/Halt only)
Trigger Enable (LE/TE)------: drive, receive.
Trigger (HE/TR)-------------: drive, receive.
Delay Clock (HE/DLCK)-------: receive only.
Storage Enable (LE/SE)------: not used.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information for installing the Model 64602A. Included are initial inspection procedures, preparation for use, and instructions for repacking the instrument for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Procedures for checking electrical performance are given in Section IV. If the contents are not complete, if there is mechanical damage or defect, or if the instrument does not pass the Performance Tests, notify the nearest Hewlett-Packard Office. If the shipping container is damaged, or if the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard Office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. PREPARATION FOR USE.

2-6. There are no specific preparation for use procedures except the actual installation of the boards in the Mainframe cardcage.

2-7. INSTALLATION INSTRUCTIONS.

WARNING

WHEN REMOVING OR INSTALLING THE TIMING ANALYZER BOARDS,
THE MAINFRAME A.C. LINE POWER MUST BE TURNED OFF.

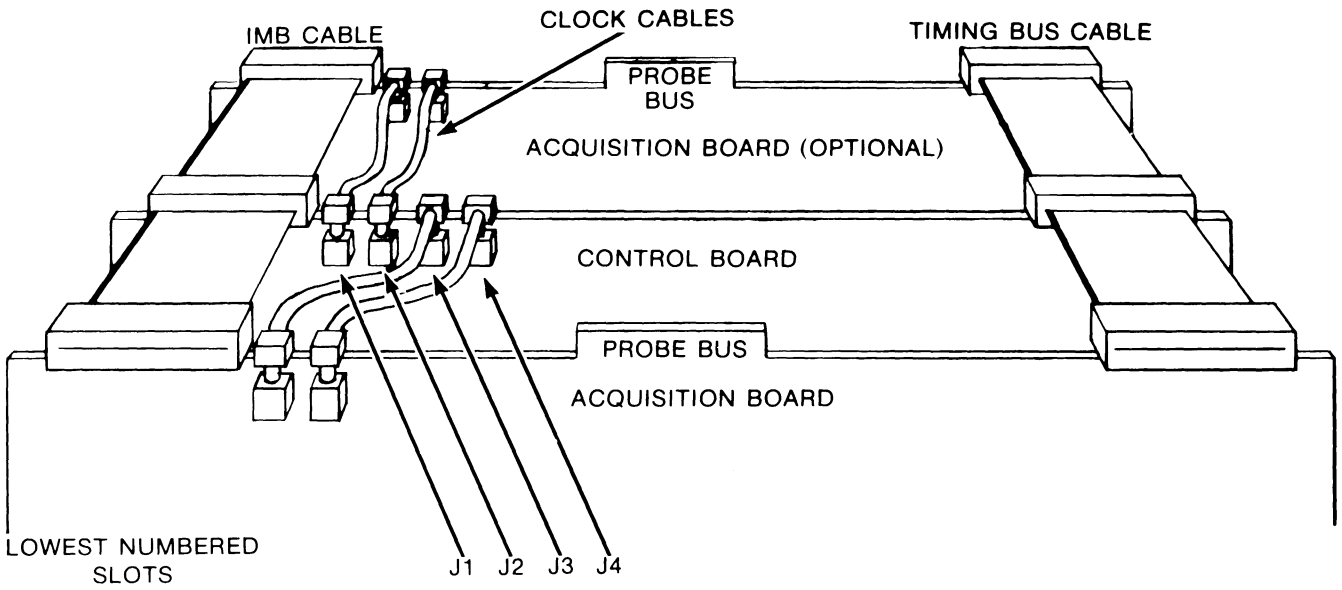

Figure 2-1. Timing Configuration

2-8. Mainframe Configuration.

2-9. Depending on the number of channels required, the timing analyzer will use two or three card slots of the mainframe cardcage.

2-10. One Timing Acquisition Board (64602A) should be installed in the lowest numbered card slot available. The Timing Control Board (64601A) then goes in the next higher slot. And if there is a second Acquisition Board, it will go in the next higher slot. In other words, Acquisition Boards are installed on either side of the Control Board. SEE FIGURE 2-1.

2-11. Up to two Acquisition Boards may be installed with one Control Board, forming one Timing Analysis Subsystem.

2-12. Inter Module Bus (IMB).

2-13. Some systems may contain a combination of a Timing Analyzer and another type of Analysis Subsystem. The Inter Module Bus, located at the upper left-hand corner of the board (when viewing from the component side) connects two or more analysis modules together for controlling and arming purposes. For example, a Timing Analyzer may arm a State Analyzer, and vice versa.

2-14. Although the 64602A has an Inter Module Bus jack, there is no electrical connection between this IMB jack and the rest of the board. The 64602A communicates with the IMB through the 64601A Timing Control Board. Since there is no electrical connection to the 64602A IMB jack and the rest of the board, this jack may have a ribbon cable connected to it for mechanical support.

2-15. Probe Bus

2-16. The timing analyzer communicates with the system under test by means of the 64604A Timing Probe. The probe cable connects to the probe bus located on the top center of the 64602A acquisition board.

2-17. Clock Cables.

2-18. Each 64602A acqusition board requires two clock inputs from the control board. Sample clocks are supplied from the control board via BNC cables connected to J1 and J2 on the upper left-hand part of the acqusition board.

2-19. Clocks should be paired: The left-hand two jacks, J1 and J2, on the control board should be connected to one acquisition board; and the right-hand two jacks should be connected to any second acquisition board.

2-20. Timing Bus.

2-21. The timing bus is at the top right-hand corner of the 64602A Acquisition Board (when viewing from the component side). The timing bus connects the timing Control Board to one or two Acquisition Boards.

2-22. The timing Control and Acquisition Boards must be grouped together to allow the timing bus ribbon cable to connect the Control Board to the Acquisition Board. When there are two Acquisition boards, which are placed on either side of the Control Board, a 3-position ribbon cable is used. Use only the timing bus cable with a part number given in the 64601A Control Board parts list. See FIGURE 2-2.

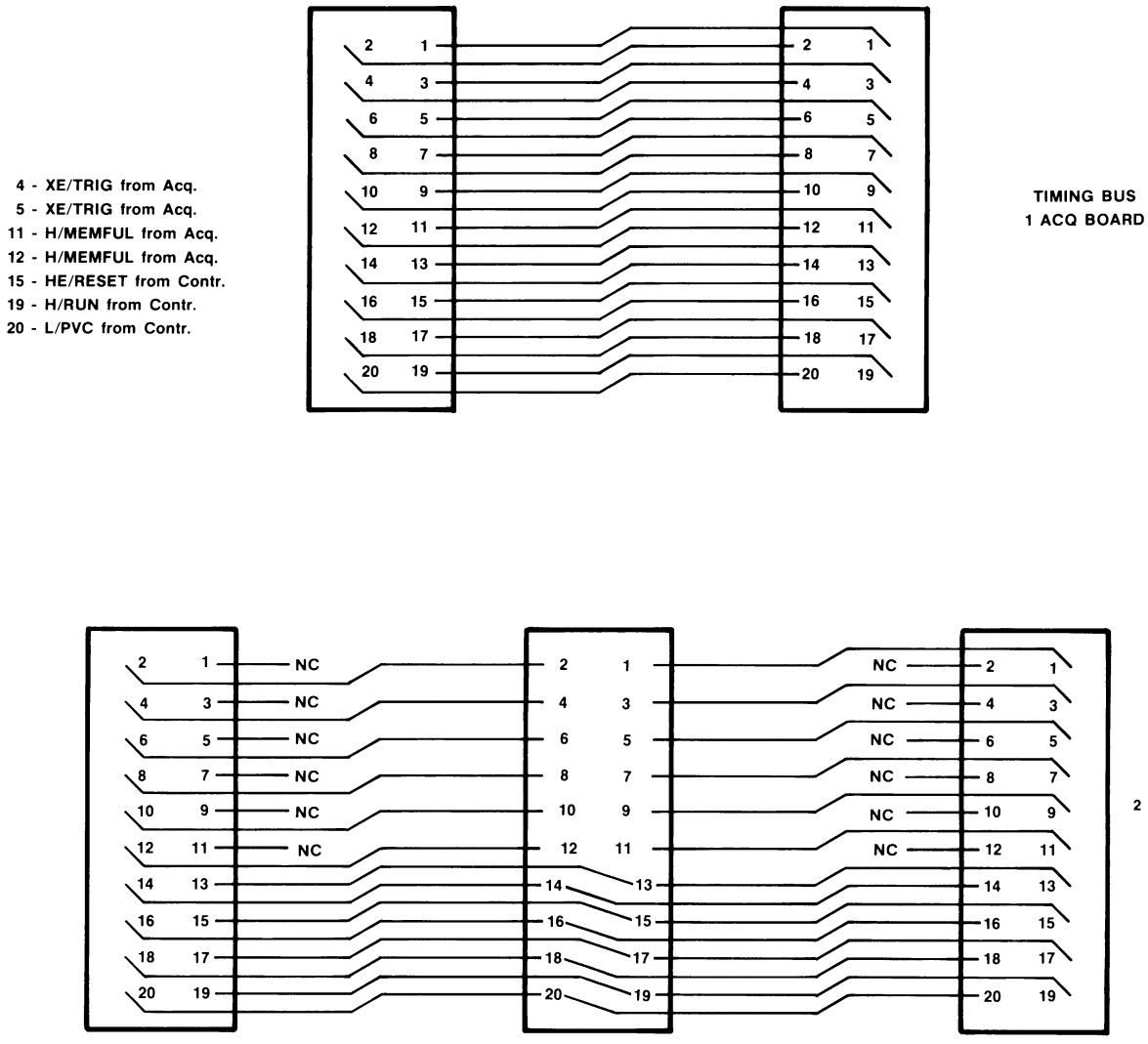

Figure 2-2. Timing Bus Cables

2-23. OPERATING, STORAGE, AND SHIPMENT ENVIRONMENTS.

CAUTION

THE GLITCH (U27) AND ENCODER (U22-25, U29-32) CHIPS ARE VERY SENSITIVE TO STATIC. THEY SHOULD BE LEFT IN CONDUCTIVE FOAM UNTIL INSTALLATION. GROUNDING STRAPS AND A GROUNDED WORK STATION ARE RECOMMENDED WHEN HANDLING THE ICS.

2-24. Operating Environment.

2-25. The Model 64602A may be operated in environments within the limits shown below. It should be protected from temperature extremes which cause condensation within the instrument.

Temperature.....+10° to +40° degrees Celsius
Humidity.....5% to 80% relative humidity
Altitude.....15 000 m (50 000 ft)

2-26. Storage Environment.

2-27. The Model 64602A may be stored or shipped in environments within the following limits:

Temperature.....-40° to +70° degrees Celsius
Humidity.....5% to 80% relative humidity
Altitude.....15 000 m (50 000 ft)

2-28. Packing.

2-29. Tagging for Service. If the instrument is to be shipped to a Hewlett-Packard Sales/Service Office for service or repair, attach a tag showing owner (with address), complete instrument repair number, and a description of the service required.

2-30. Original Packing. Containers and materials identical to those used in factory packing are available through Hewlett-Packard Offices. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and complete repair number.

2-31. Other Packing. The following general instructions should be used for repacking with commercially available materials:

a. Wrap instrument in heavy plastic or paper. (If shipping to Hewlett-Packard Office or Service Center, attach a tag indicating type of service required, return address, model number, and complete repair number.

b. Use a strong shipping container. A double wall carton made of 350 pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inches) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and complete repair number.

SECTION III

OPERATION

The operation of the Model 64602A is a function of the system software. Complete system keyboard operation is beyond the scope of the service manual. Please refer to the operator's manual (64601-90903) for the procedure.

NOTES

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PERFORMANCE TESTS

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4-2. INTRODUCTION.

4-3. Performance verification tests check the major circuit blocks for proper operation, giving the operator at least 90% confidence that the board is operating correctly.

4-4. There are 9 PV Tests and 2 Supplementary Tests. The supplementary tests use different access instructions. They are described after the the regular 9 PV tests.

4-5. Signature analysis instructions and tables are given at the end of the section.

4-6. The performance verification tests are also used in troubleshooting: (1) They help to isolate troubles to particular blocks, and within particular blocks; (2) Each test corresponds to a one signature loop when running signature analysis.

4-7. Each test is shown on the mainframe screen as a bracket group of 0's. The 0's correspond to steps in a particular test. When the board fails a test step, the "0" for that step becomes a "1".

4-8. TROUBLESHOOTING TECHNIQUES.

4-9. Although each of the PV tests checks a specific circuit block, signals from other blocks are used. A failure in one block can be caused by failures in blocks upstream. The following steps are suggested for troubleshooting.

4-10. Check board seating.

4-11. Check cable connections.

All cables should be fastened securely. The clock cables should be paired on the left or right two jacks. The timing bus and IMB cables should have the pin 1 wire connected to pin 1 on the jack. No cables other than the two listed in the 64601A Control Board manual parts list may be used for the timing bus.

4-12. Check supply voltages.

Supply voltages from the mainframe (+5V, -5.2V, -12V) should be within 5%. The -3.25V should be within 3%.

4-13. Isolate the problem to one board.

When a PV failure occurs, isolate the problem to either an acquisition board, or the control board. Check signatures on the timing bus, which connects the control board to the acquisition board(s). Look first at the signals HE/RUN and HE/RESET from the control board. If these are good, look at the return signals from the acquisition board(s), H/MEMFUL, XE/TRIG1(2). In a two-acquisition board system, H/MEMFUL comes from the acquisition board in the lower numbered slot only.

4-14. Check the programming.

In PV tests the mainframe stimulates the timing analyzer and verifies correct operation by looking at the status registers. Read each test description to see what is being stimulated. Look at the signatures on the outputs of address decoders, data latches, and mode registers where the mainframe is stimulating that PV test circuit block. Correct signatures may be traced back to where signals become incorrect.

4-15. Check the status registers.

A PV failure means the status registers for the acquisition board on service sheet 5 will have one or more incorrect output signatures. The signal path may then be traced back to the problem.

4-16. PHYSICAL SETUP CONDITIONS FOR THE PV TESTS.

4-17. Conditions for the following tests:

a. Connect the timing pod to the 64602A acquisition board by means of timing cable 64604-61601.

b. Leave the probe leads disconnected, so that the probe inputs are floating near ground.

c. Make sure the two clock cables are securely connected. Clock cables should be connected in pairs to either the two right or two left jacks of the 64601A control board.

d. The timing bus cable should be connected to the jacks at the upper right hand corner (when viewing from the component side) of both the 64601A control board and the one or two 64602A acquisition board(s). Only timing bus cables (two or three position) listed in the 64601A parts list should be used.

e. NOTE: In noisy environments, ground each probe input, using the ground lead for each probe. Failure to do this may result in the PV displaying intermittent, non-existent failures.

CAUTION

THE GLITCH (U27) AND ENCODER (U22-25, U29-32) CHIPS ARE VERY SENSITIVE TO STATIC. THEY SHOULD BE LEFT IN CONDUCTIVE FOAM UNTIL INSTALLATION. GROUNDING STRAPS AND A GROUNDED WORK STATION ARE RECOMMENDED WHEN HANDLING THE ICS.

4-18. KEYBOARD SETUP (For running all nine PV tests repeatedly).

4-19. To verify that the entire board is operating correctly, perform the following steps on the mainframe keyboard:

a. With the operating system initialized and awaiting a command, press the softkey labeled "opt_test" (you may have to keep pressing the "etc" softkey until you see "opt_test" on the screen). Or you may type "option_test" in lower case.

b. Press [RETURN]. You should see a listing of all the optional boards that are present in your mainframe, along with their slot numbers.

c. Type in the Timing Acquisition Board slot number.

d. Press [RETURN].

e. Press softkey "run".

f. Press softkey "slot".

g. Type in the Timing Acquisition Board slot number.

h. Press softkey "repeated".

i. Press [RETURN]. As shown in Figure 4-1, the screen will now show all 9 Acquisition Board PV tests. Tests that pass will be indicated by "0", and failures will be indicated by "1". The screen will also show the number of times the tests are run, and the number of failures.

j. When finished with the test, press the "stop" softkey.

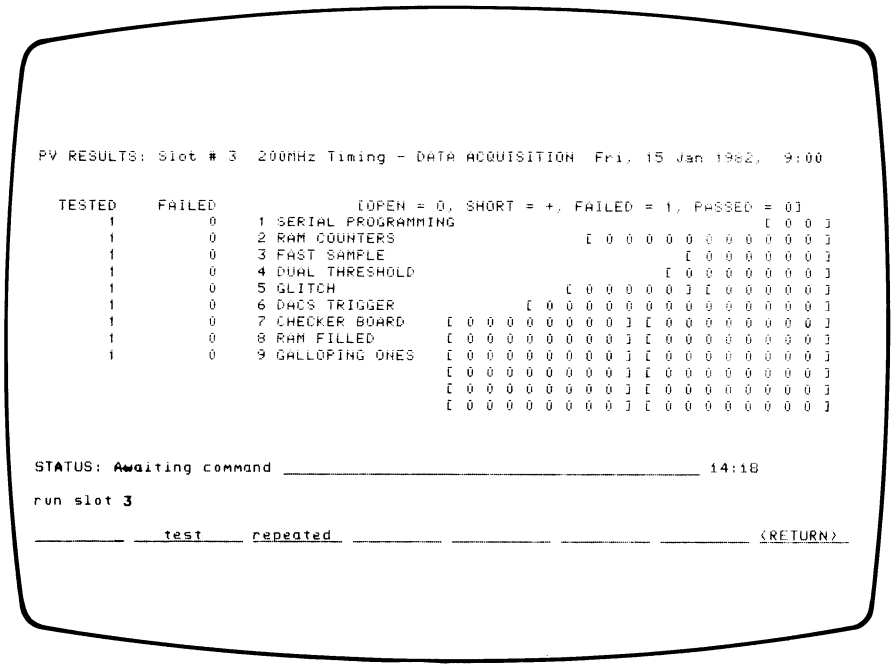

Figure 4-1. Display of PV Tests.

4-20. KEYBOARD SETUP (For running one PV test repeatedly).

4-21. To run one test at a time repeatedly for signature analysis, perform the following steps: (See Figures 4-2 to 4-10)

a. Press softkey "opt_test"; RETURN.

b. Type in the Timing Acquisition Board slot number; RETURN.

c. Press softkey "run".

d. Press softkey "slot".

e. Type in the Timing Acquisition Board slot number.

f. Press softkey "test". The screen will now list all

g. the Timing Acquisition Board PV tests.

h. Type in the number of the test you wish to run.

i. Press the soft key "repeated".

j. Press [RETURN].

4-22. EXPLANATION OF THE TEST DESCRIPTIONS.

4-23. There are 9 performance verification tests for the Timing Acquisition Board. Each of these tests has one or more TEST STEPS, denoted by the 0's or 1's within brackets. A "0" in the bracket indicates a PASS for that test step; and a "1" indicates FAIL.

1. SERIAL PROGRAMMING	[00]
2. RAM COUNTERS	[00000000000]
3. FAST SAMPLE	[000000]
4. DUAL THRESHOLD	[0000000]
5. GLITCH	[00000][00000]
6. DACS TRIGGER	[00000000000000]
7. CHECKER BOARD	[00000000][00000000]
8. RAM FILLED	[00000000][00000000]
9. GALLOPING ONE'S	[00000000][00000000]
	[00000000][00000000]
	[00000000][00000000]
	[00000000][00000000]

4-24. The numbered TEST STEPS described in each PV test correspond, from left to right, to the 0's or 1's within the displayed brackets.

4-25. The numbered TEST STEPS describe the commands given by the system software. They do not call for operator intervention.

4-26. TEST 1: SERIAL PROGRAMMING [0 0]

test steps: 1 2

4-27. Purpose. This test checks the glitch chip (U27) programming.

4-28. Test Steps. (Description of software execution)

1. The 20-bit glitch chip holding register is loaded with all HIGHs and a single LOW is walked through. After 20 clocks, nineteen HIGHs and one LOW should have appeared at the holding register output (U27-8).

2. The holding register is loaded with all LOWs and a single HIGH is clocked through. After 20 clocks, a HIGH should appear at U27-8.

4-29. D/A Converter Adjustment.

This test will also allow adjustment of the -FS(full scale) pot for the D/A converters. The -FS, +FS1, and +FS2 pots are located together at the top of the board.

See Section 5 for the adjustment procedure.

4-30. TEST 2: RAM COUNTERS [0 0 0 0 0 0 0 0 0 0 0 0]

test steps: 1 2 3 4 5 6 7 8 9 10 11

4-31. Purpose. This test checks memory-address-counter clocking and counting.

4-32. Test Steps. (Description of software execution)

1. Analyzer is reset. The X-counters should read 00H. (Y-counters cannot be read directly). H/MEMFUL should be false.

2. Memory Address Counters are set to AAH (AAx and AAy).

3. X-counter is clocked to FFH. (Since the Y-counter is behind, at most, by one clock, it will be at FFH or FEH).

4. X-counter is clocked once more. It should read 00H.

5. Analyzer is clocked to one before the memory is full. Both X and Y counters should be 01H. H/MEMFUL should still be false.

The wrap-around latch (U4) sends H/MEMFUL to the mainframe processor when the memory address counters overflow for the first time during acquisition. H/MEMFUL will continue true from then on, no matter how many times the counters go around, until the analyzer is RESET. Thus, the counters indicate when memory has been filled with new data at least once.

6. Clock once more. H/MEMFUL should be high. This indicates indirectly that the Y-counter has been counting correctly.

7. Reset, and set the memory address to 55H (55x and 55y). H/MEMFUL should be low.

8. X-counter is clocked to FFH.

9. X-counter is clocked once more. It should read 00H.

10. Analyzer is clocked to one before the memory is full. Both X and Y counters should be 01H. H/MEMFUL should still be false.

11. Clock once more. H/MEMFUL should be high.

4-33. D/A Converter Adjustment.

After test #2 (ram counters) is run, the DACs are left with +2.117V (+/- 7.0mV) on TP1 and TP2. Adjustments may be made using the procedure in Section 5.

4-34. TEST 3: FAST SAMPLE TEST [0 0 0 0 0 0]

test steps: 1 2 3 4 5 6

4-35. Purpose.

This test verifies that the counters are running, that clocks are getting through the system, and that the fast sample latch (U71B) sets and resets. The following conditions are programmed: fast sample mode is set; glitch chip is programmed to never trigger.

4-36. Test Steps. (Description of software execution)

1. Reset and turn on the Fast Sample Mode. H/MEMFUL should be false.
2. The fast sample latch should be set.
3. Start acquisition. H/MEMFUL should go true.
4. Reset and turn on the Wide Sample Mode/200MHz. H/MEMFUL should be false.
5. The fast sample latch should be reset.
6. Start acquisition. H/MEMFUL should go true.

4-37. D/A Converter Verification.

After test #3 (fast sample) is run TP1 and TP2 should show 0V (+/- 4.5mv). This test is for Verification only. See Section 5 for the adjustment procedure.

4-38. TEST 4: DUAL THRESHOLD MODE [0 0 0 0 0 0 0]

test steps: 1 2 3 4 5 6 7

4-39. Purpose.

This test exercises the timing probe, the glitch chip (U27), the two D/A converters (DACs), and the dual threshold latch (U71A) in the Dual Threshold Mode.

4-40. Theory.

In the Dual Threshold Mode, DAC A (U76) sets the lower threshold, using channels 0-3; and DAC B (U78) sets the upper threshold, using channels 4-7.

Since two channels are needed for each probe input, an analyzer with only one acquisition board is reduced to four channels. Only the low order probe inputs--0,1,2,3--are active.

Each of these low order probe inputs comes into the board on two separate channels: probe 0 => channels 0 & 4, probe 1 => channels 1 & 5, probe 2 => channels 2 & 6, and probe 3 => channels 3 & 7.

Since one of the set-up conditions for the PV tests is that the probes are left disconnected and floating near ground, incoming data levels are simulated by varying the DAC thresholds: a HIGH probe input is simulated by a LOW threshold.

The dual threshold mode is set by the dual threshold latch (U71A), which sends HE/DT to the probe bus (J1-22). HE/DT is used to latch the probe pod into the dual threshold and fast sample modes. In both of these modes, only four probe inputs are active.

4-41. Test Steps. (Description of software execution)

1. The dual threshold latch, U71A, is reset.

2. The dual threshold latch is set.

TEST 4: DUAL THRESHOLD MODE (continued)

In each of the next five tests, the DACs are exercised in all of the following ways:

a. Both thresholds are set to maximum (+12.7V): all probe data will be seen as LOW.

b. Both thresholds are set to minimum (-12.8V): all probe data will be seen as HIGH.

c. Upper thresholds are set to +12.7V, and lower thresholds are set to -12.8V.

d. Upper thresholds are set to -12.8V, and lower thresholds are set to +12.7V.

e. DACs are set back to condition "a".

3. Program the glitch chip to always trigger. XE/TRIG should be true under all the above conditions.

4. Program the glitch chip to trigger only on a HIGH. XE/TRIG should be true only under condition b.

5. Program the glitch chip to trigger only on a selected middle level. Trigger should occur only under condition d.

6. Program the glitch chip to trigger only on a LOW. Trigger should occur only under condition a.

7. This step checks that XE/TRIG and XE/TRIGPOL to the status register U82 were the correct polarity in all the above tests.

4-42. D/A Converter Adjustment Verification.

After test #4 (dual threshold) is run, the DACs are left with TP1=+1.666 and TP2=-1.666 (with the probes disconnected). THIS TEST IS FOR VERIFICATION ONLY!. Adjustments are made using test #1 and test #2.

4-43. TEST 5: GLITCH MODE TEST

	[0 0 0 0 0] [0 0 0 0 0]
test steps:	1 2 3 4 5 6 7 8 9 10

4-44. Theory.

Glitches are defined as two or more transitions between sample times.

When the DAC thresholds are set HIGH or LOW, it makes inputs from the floating probes appear to be at the opposite level. In this test the DAC thresholds are "wiggled" between clock edges to create glitches.

4-45. Purpose.

This test exercises the probe and glitch chip (U27) in the glitch mode. The test verifies a trigger (XE/TRIG at U82-4) under the following conditions:

a. The sample clock begins with a leading edge. That is, the first sample time corresponds to a leading clock edge.

b. The sample clock begins with a trailing edge.

c. Glitch transitions, between sample times, begin with a leading edge.

d. Glitch transitions begin with a trailing edge.

e. Two glitch transitions occur between clock edges.

f. Three glitch transitions occur between clock edges.

4-46. Test Steps. (Description of software execution)

In the first bracket group, the sample clock alternates HIGH-LOW-HIGH. Each test covers a sequence, starting and ending with the the clock HIGH.

1. The Glitch Mode is set. No trigger (XE/TRIG=1 at U82-4) should occur on a normal data transition.

2. Two glitch transitions, beginning with a falling edge, occur between samples: XE/TRIG = 1.

3. Three glitch transitions occur, beginning with a falling edge: XE/TRIG=1.

4. Two glitch transitions occur, beginning with a rising edge: XE/TRIG=1.

5. Three glitch transitions occur, beginning with a rising edge: XE/TRIG=1.

GLITCH MODE TEST (continued)

In the second bracket group, the clock alternates LOW-HIGH-LOW.

6. No trigger on a normal data transition.

7. XE/TRIG = 1 after two transitions which begin on a falling edge.

8. Triggers on three transitions which begin on a falling edge.

9. Triggers on two transitions which begin on a rising edge.

10. Triggers on three transitions which begin on a rising edge.

4-47. D/A Converter Adjustment Verification.

After test #5 (glitch mode) is run, the DACs are left with TP1=-1.666 and TP2=+1.666 (with the probes disconnected). THIS TEST IS FOR VERIFICATION ONLY! Adjustments are made using test #1 and test #2.

4-48. TEST 6: DACS TRIGGER TEST

	[0 0 0 0 0 0 0 0 0 0 0 0 0 0]
test steps:	1 2 3 4 5 6 7 8 9 10 11 12 13 14

4-49. Purpose.

This test checks the D/A converters, the probes, and the glitch chip.

4-50. Test Steps. (Description of software execution)

In each of the following tests, the DACs are exercised as in the DUAL THRESHOLD TEST above.

1. The glitch chip is programmed to always trigger. XE/TRIG should be true under all the conditions given in the DUAL THRESHOLD TEST.

2-9. The glitch chip is programmed so that one channel at a time will never trigger. In other words, a "never-trigger" is walked through all the channels, and the thresholds are exercised under all conditions. XE/TRIG (U82-4) should be false for all these tests.

10. The glitch chip is programmed so that all channels will trigger on a HIGH. XE/TRIG should be true only under condition b, as given in the Dual Threshold Test.

11. The glitch chip is programmed so that all channels will trigger on a LOW. XE/TRIG should be true only under condition a.

12. Channels 0-3 are programmed with a LOW threshold, and channels 4-7 are programmed with a HIGH threshold. XE/TRIG should be true only under conditon c.

13. Channels 0-3 are programmed with a HIGH threshold, and channels 47 are programmed with a LOW threshold. XE/TRIG should be true only under condition d.

14. For all the above tests, XE/TRIG to the timing bus was true at the correct times.

4-51. TEST 7: CHECKER BOARD

test steps:	1	2
	[0 0 0 0 0 0 0 0]	[0 0 0 0 0 0 0 0]
RAM channels:	0 7 1 6 2 5 3 4	0 7 1 6 2 5 3 4

4-52. Purpose.

This test checks the RAMs and the output stage of the encoders by loading two alternating patterns of HIGHs and LOWs into each memory channel, and then verifying. The patterns are generated by the pattern generator inside the encoders.

A memory channel consists of the four RAMs loaded by a particular probe channel in the Wide Sample Mode.

Each "0" in a bracket corresponds to a memory channel in the following order: 0,7,1,6,2,5,3,4.

4-53. Test Steps. (Description of software execution)

1. Load 01010101... into memory channels 1,2,5,6; and 10101010... into memory channels 0,3,4,7. The RAM looks like one big checker board. All locations are tested.

2. Load 10101010... into memory channels 1,2,5,6; and 010101... into channels 0,3,4,7. This is the same as the previous test except that all bits are complemented.

4-54. TEST 8: RAM FILLED

test steps:	1	2
	[0 0 0 0 0 0 0 0]	[0 0 0 0 0 0 0 0]
RAM channels:	0 7 1 6 2 5 3 4	0 7 1 6 2 5 3 4

4-55. Purpose.

This test checks the acquisition RAM by loading in all HIGHs or all LOWs, and then verifying.

A "memory channel" consists of four RAMs that correspond to a particular probe channel in Wide Sample Mode.

Each "0" in a bracket corresponds to a memory channel in the following order: 0,7,1,6,2,5,3,4.

4-56. Test Steps. (Description of software execution)

1. By programming the DAC thresholds for a maximum positive value, load all LOWs into memory channels 0-7, and verify. All locations are tested.

2. By programming the DACs with a maximum negative threshold, load all HIGHs into RAM channels 0-7. All locations are tested.

4-57. TEST 9: GALLOPING ONE'S [00000000][00000000]
[00000000][00000000]
[00000000][00000000]
[00000000][00000000]

This test checks address lines, rather than memory itself. The bracket GROUPs represent address lines, or bits. (Since the X and Y addresses are identical for this test, only eight address bits, corresponding to a 16-bit location, are needed.) The "0's" in each group represent memory channels in the order: 0,7,1,6,2,5,3,4. Thus:

A0 A1
[chs.0,7,1,6,2,5,3,4] [chs.0,7,1,6,2,5,3,4]

A2 A3
[chs.0,7,1,6,2,5,3,4] [chs.0,7,1,6,2,5,3,4]

A4 A5
[chs.0,7,1,6,2,5,3,4] [chs.0,7,1,6,2,5,3,4]

A6 A7
[chs.0,7,1,6,2,5,3,4] [chs.0,7,1,6,2,5,3,4]

4-58. Procedure used by the software in this test.

After clearing memory, load FFFFH into the same 16-bit address in all channels. Read that location in each channel. Then read the memory. If only the location corresponding to the exercised address bit contains FFFFH, no address lines are open or shorted.

Addresses are chosen in the following way: One address bit at a time is first made LOW, then HIGH. The corresponding power-of-two addresses will then be: 01H,...,08H and FEH,...,7FH, as follows:

HEX ADDR.	ADDR. LINES A7	A6	A5	A4	A3	A2	A1	A0	CHANNELS: 0,7,1,6,2,5,3,4
01	L	L	L	L	L	L	L	H	EACH
02	L	L	L	L	L	L	H	L	EACH
04	L	L	L	L	L	H	L	L	EACH
08	L	L	L	L	H	L	L	L	EACH
10	L	L	L	H	L	L	L	L	EACH
20	L	L	H	L	L	L	L	L	EACH
40	L	H	L	L	L	L	L	L	EACH
80	H	L	L	L	L	L	L	L	EACH
and then:									
FE	H	H	H	H	H	H	H	L	EACH
FD	H	H	H	H	H	H	L	H	EACH
FB	H	H	H	H	H	L	H	H	EACH
F7	H	H	H	H	L	H	H	H	EACH
EF	H	H	H	L	H	H	H	H	EACH
DF	H	H	L	H	H	H	H	H	EACH
BF	H	L	H	H	H	H	H	H	EACH
7F	L	H	H	H	H	H	H	H	EACH

GALLOPING ONE'S (continued)

For example, when bit A0 is exercised:

a. Address 01H should be the only location in all channels to contain FFFFH.

b. Then address FEH should be the only location in all channels to contain FFFFH.

c. If both of these conditions are true, the first bracket will contain only "0's".

The following inferences can be made from this test:

a. If the selected address does not contain FFFFH, that address line is open and will be indicated by one or more "O"s instead of "0's".

b. Two or more address lines are shorted if any of the other addresses also contain FFFFH. For example, when exercising 01H, if 09H also contains FFFFH, then A0 is shorted to A3. This will cause "1" to appear on all channels of those two address lines, eg: [11111111] [11111111].

c. A RAM internal short, after the input buffers, may appear as a "+" on one of the channels, eg: [0000+000], indicating channel 2. Since a memory channel is composed of four RAMs, the problem can then be narrowed down to one of four RAMs.

d. The encoders or glitch chip may also cause failures to occur in this test, even though previous tests have passed. For example, if both the X and Y addresses are the same, except for A0, and the signatures are correct on the address lines, check the signatures on the outputs of the RAMs. If these are correct, but one or more of the input data line signatures are wrong, the problem is likely to be the encoder for that channel.

4-59. SUPPLEMENTARY BOARD ID TEST

4-60. The board ID circuits have stable signatures when "opt_test" is pressed. If the Timing Boards are not then listed on the screen, the ID circuitry is not working. Check the ID circuitry signatures (U75, U82).

4-61. SUPPLEMENTARY PV SKEW TEST.

4-62. The Skew Test is a supplementary PV test which checks the skew between channels.

4-63. Skew is the difference in delay between any two channels.

4-64. There are two stages to the skew test. In the first stage one of the eight probe channels is chosen as a reference channel, and either one or all of the other seven channels is measured for skew against the reference.

4-65. The second stage of the test is done in the fast sample mode. This test measures the amount of skew in the two channels paired in the fast sample mode. If the first stage test measured 0.0 ns skew for these two channels, the skew now measured in the Fast Sample Delay Line test should be exactly 2.5 ns, which is the delay caused by the fast sample delay line.

4-66. To access the Skew Test, perform the following:

1. Press "opt_test". RETURN.
2. Type in the slot number for either the timing control or acquisition boards. RETURN.
3. Type in "skew". RETURN.
4. The screen should now display the setup information for the skew test as shown in figure 4-2.

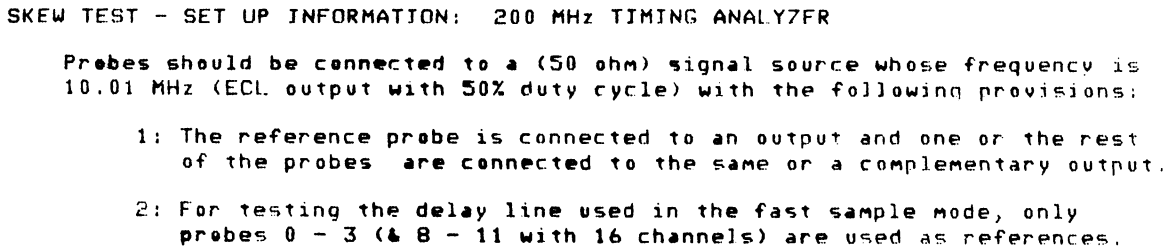

Figure 4-2. Skew Test Setup

4-67. To perform the first skew test:

1. Press "skew_test".

2. You may now choose a reference channel, and then press RETURN.

3. If you don't choose a reference channel, the system will automatically select channel 0.

4. When you press RETURN, the display will show the skew of all the other channels with respect to the reference channel, using both positive and negative edges. (SEE FIGURE 4-3). The test cycles 25 times and lasts about one and three-quarter minutes.

5. The amount of skew shown in this test when the probe is connected properly according to the setup conditions shown in the first display should be 1.5 ns typical.

200 MHz TIMING: Nano Seconds of SKEW - with respect to
POSITIVE EDGES: NEGATIVE EDGES: of the reference channel's signal

CHANNEL:	0	ref		ref
	1	0.0ns		0.0ns
	2	0.0ns		0.0ns
	3	0.0ns		0.0ns
	4	0.0ns		0.0ns
	5	0.0ns		0.0ns
	6	0.0ns		0.0ns
	7	0.0ns		0.0ns

Figure 4-3. First Skew Test

4-68. To perform the second skew test:

1. Press "fast_samp"

2. The screen will display "fast_sample_delay _line _test".

3. You may now either choose a reference channel, or let the system default to channel 0.

4. Press RETURN. The screen will show the amount of skew in the channel paired in the fast sample mode with the reference channel. For example, if channel 0 is the reference channel, channel 4 will be the other channel used in the measurement because channel 4 is paired with channel 0 in the fast sample mode. Similarly, channels 1 and 5, channels 2 and 6, and channels 3 and 7 will be paired. (SEE FIGURE 4-4).

5. The amount of skew shown in this test when the probe is connected properly according to the setup conditions shown in the first display should be 2.5 ns **typical, which is the length of the delay line.**

```
200 MHz TIMING: Nano Seconds of FAST SAMPLE DELAY-LINE-SKEW (2.5nS Typ.)
     POSITIVE EDGES:   NEGATIVE EDGES: of the reference channel's signal
CHANNEL: 0    ref              ref
         1
         2
         3
         4    0.0ns            0.0ns
         5
         6
         7
```

Figure 4-4. Second Skew Test

4-69. PV SOFTKEY SEQUENCE.

The following figures (4-5 to 4-13) show the softkey sequence needed to run a single PV test repeatedly for signature analysis. Each PV test corresponds to one signature loop. The signature lists are given after the figures.

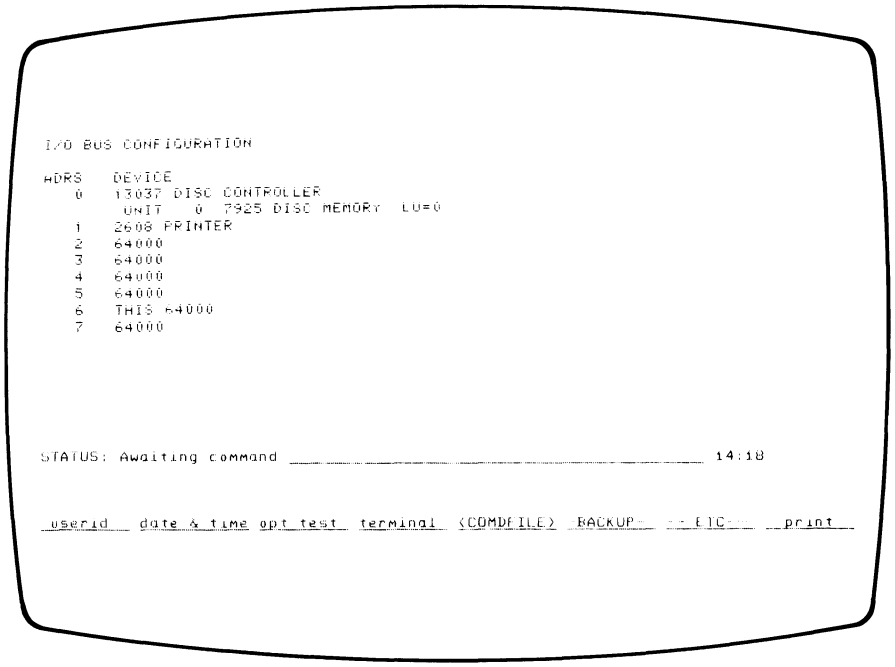

Figure 4-5. Press "opt_test".

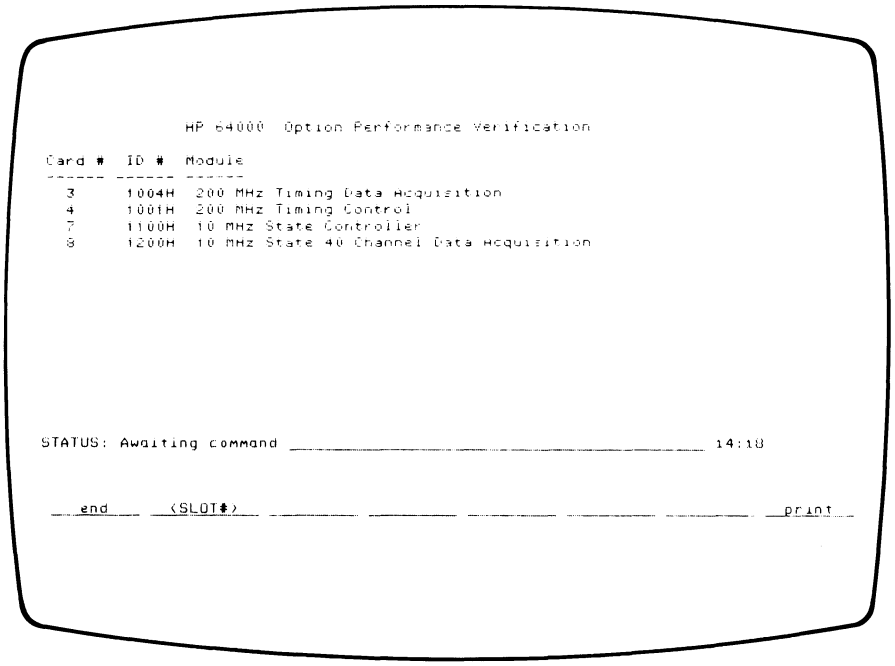

Figure 4-6. Type the slot number.

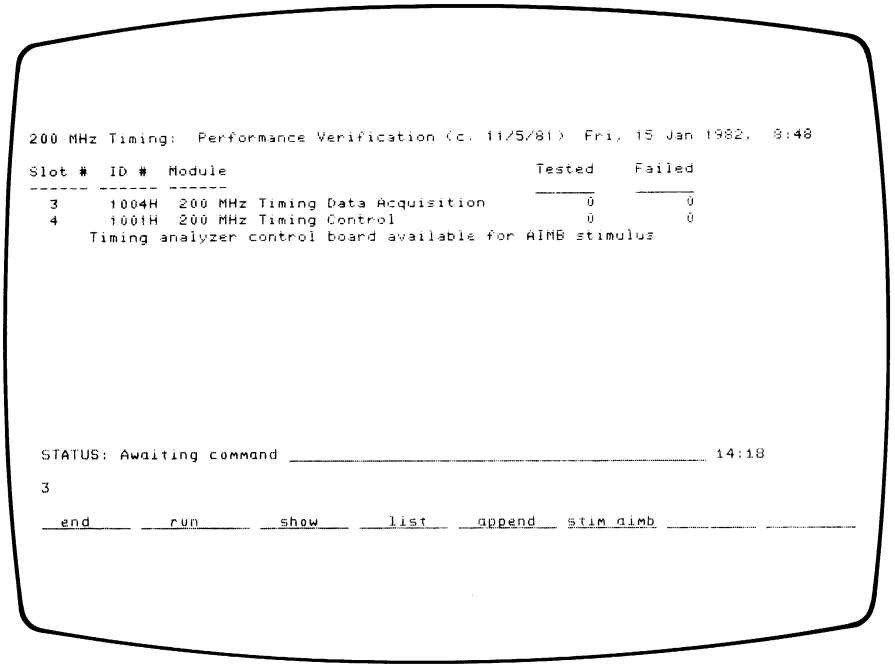

Figure 4-7. Press "run".

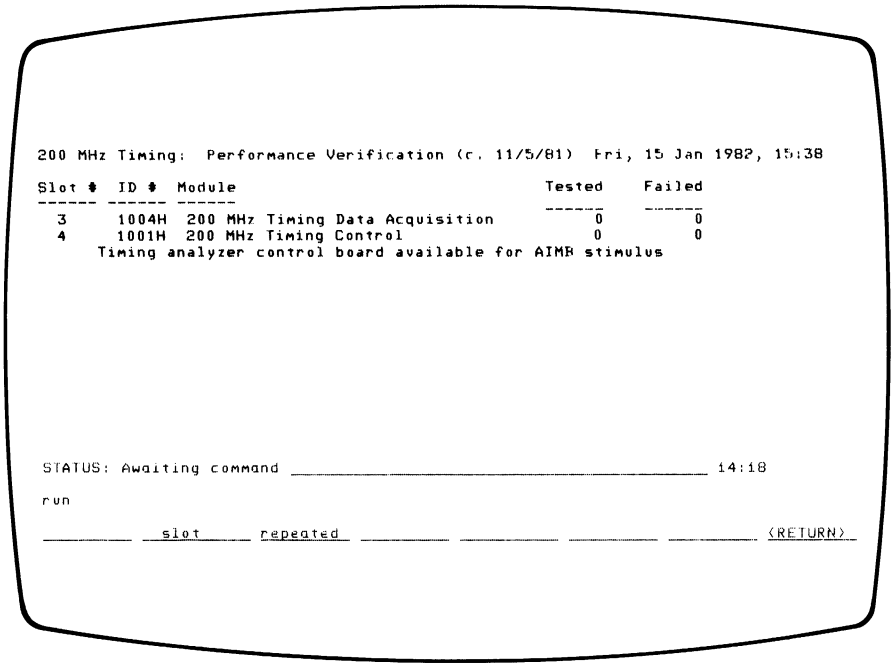

Figure 4-8. Press "slot".

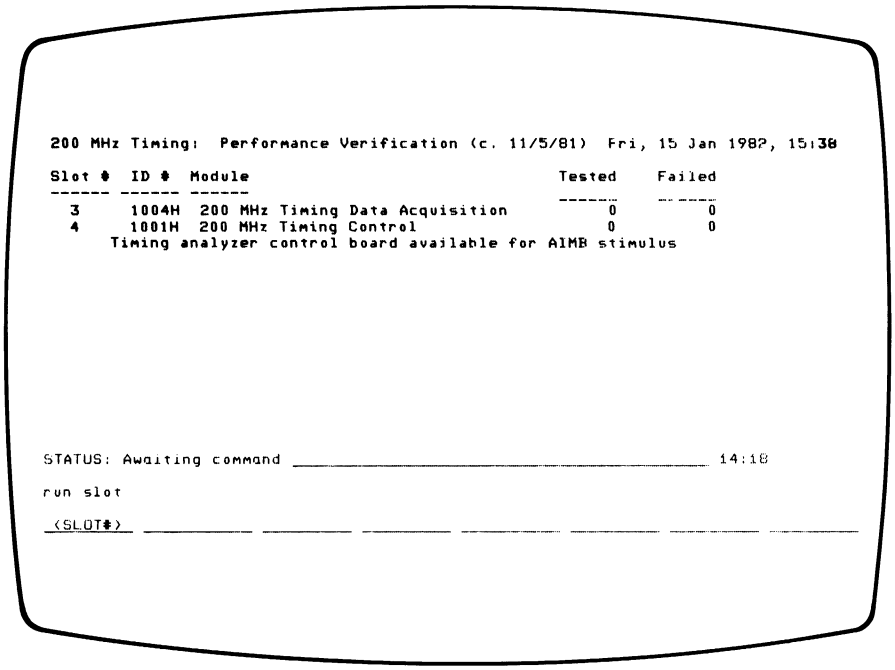

Figure 4-9. Type the slot number.

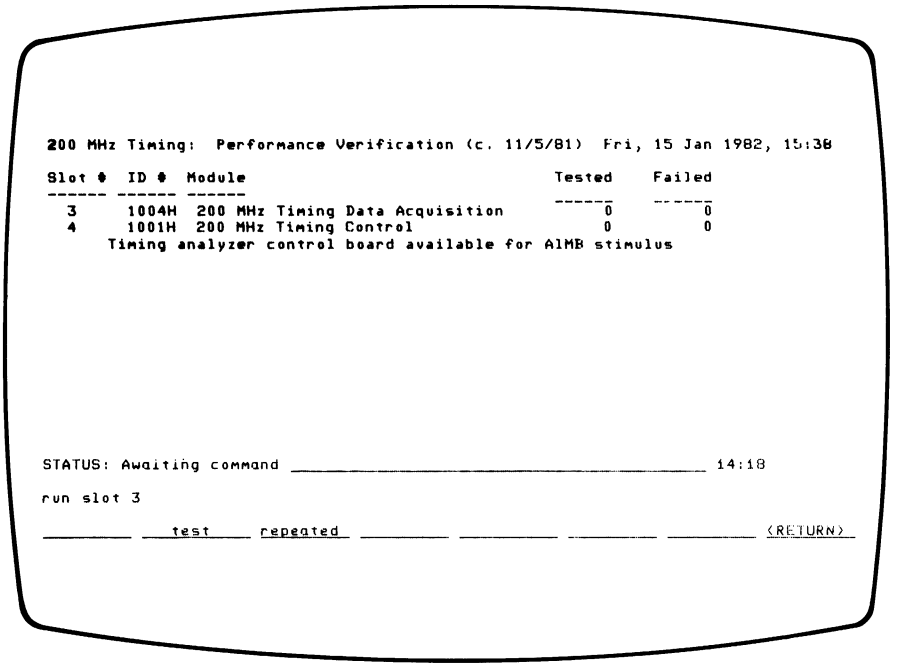

Figure 4-10. Press "test".

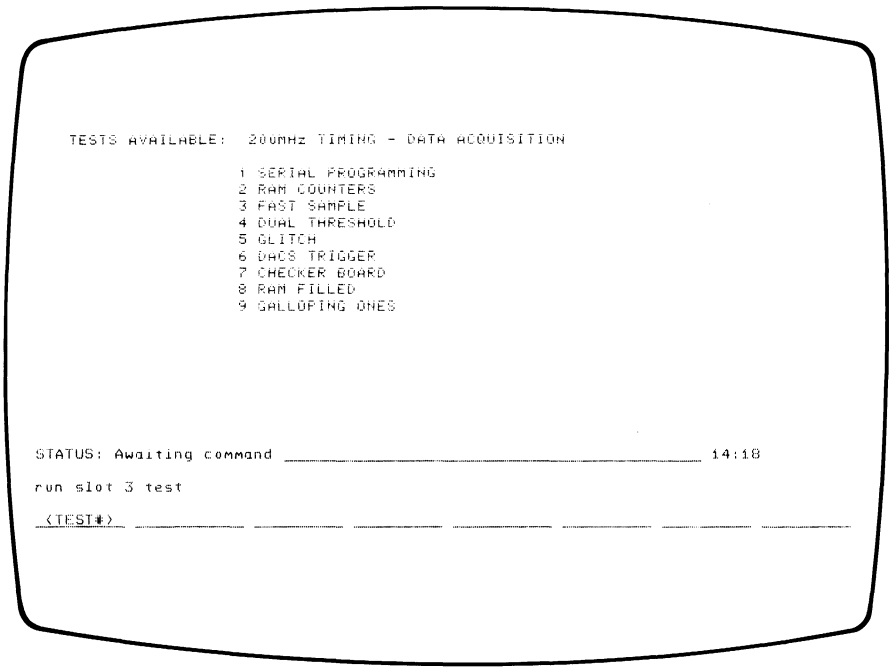

Figure 4-11. Type the test number.

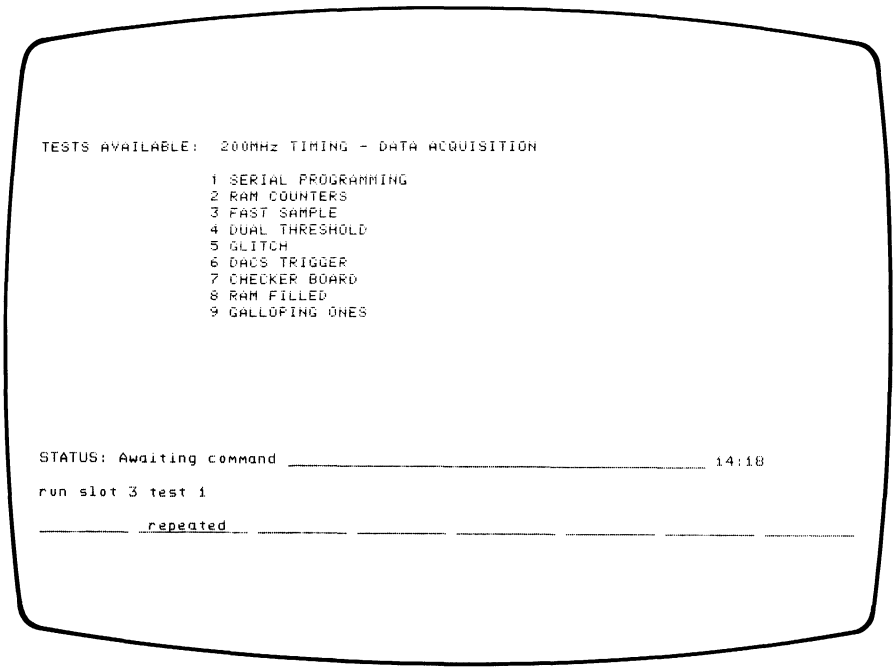

Figure 4-12. Press "repeated".

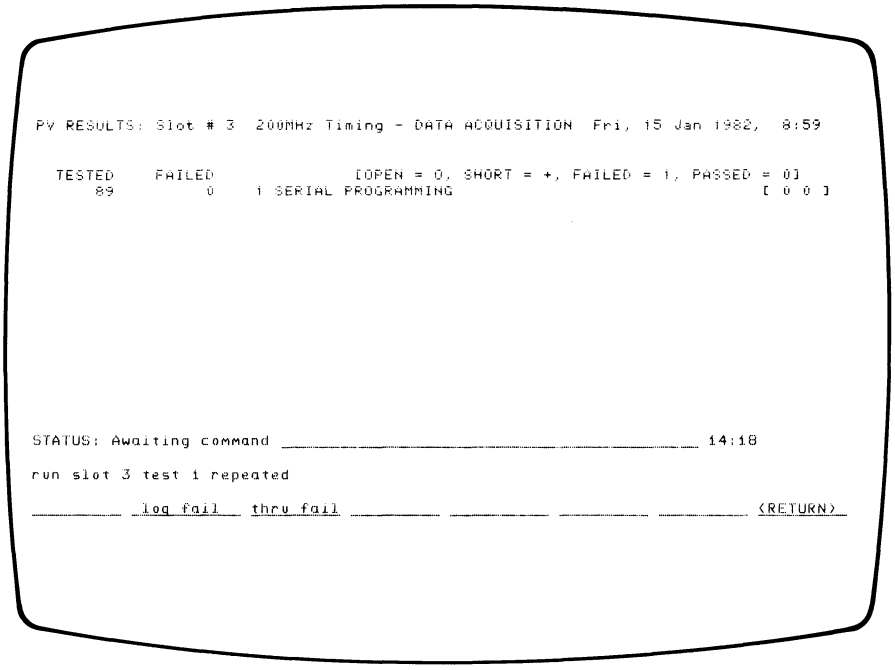

Figure 4-13. Press [RETURN].

4-70. SIGNATURE ANALYSIS.

4-71. The following 9 signature loops correspond to the previously given performance verification tests. That is, if a PV test fails, run the signature loop corresponding to that test. For example, if one of the test steps for TEST 1: SERIAL PROGRAMMING shows a "1" instead of a "0" in the bracket, look at the signatures for LOOP 1. In order to take the signatures, run TEST 1 repeatedly, using the procedure illustrated by the above figures (4-2 to 4-10).

64602A Timing Acquisition Board
SERIAL PROGRAMMING #1

NORM MODE VH = CC7A

DATA THRESHOLD: ecl & ttl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: sa gate neg. edge
Location of QUAL/STOP: sa gate pos. edge
Location of CLOCK: sa clk pos. edge
Location of GROUND: gnd

ECL

U 7-13	7524
U 7-15	FP5P
U 11-13	7524
U 16-11	9UA5
U 16-15	8808
U 17- 2	9UA5
U 17- 3	AFH7
U 17- 5	8808
U 27- 1	low
U 27- 2	high
U 27- 3	596F
U 27- 4	low
U 27- 5	high
U 27- 6	596F
U 27- 8	8808
U 27- 9	high
U 27-10	FP5P
U 27-12	0000
U 27-13	high
U 27-14	0000
U 27-15	high
U 27-16	high
U 27-17	low
U 27-18	high
U 27-19	high
U 27-20	low
U 27-21	high
U 27-22	high
U 27-23	low
U 27-24	high
U 27-25	high
U 27-26	low
U 27-27	0000
U 27-28	high
U 27-29	0000
U 27-31	AFH7
U 27-32	high
U 27-33	low
U 27-34	high
U 27-35	low
U 27-36	high
U 27-37	596F
U 27-38	low
U 27-39	high
U 27-40	596F

TTL

U 11-11	FP5P
U 16-12	9UA5
U 16-13	8808
U 70- 1	low
U 70- 4	HHCH
U 70- 5	870C
U 70- 6	CC7A
(TOTLZ=0161)	
U 70- 7	870C
U 70- 9	870C
U 70-11	high
U 70-13	high
U 70-14	0000
(TOTLZ=0161)	
U 70-15	high
U 70-16	HHCH
U 70-19	A899
U 72- 1	high
U 72- 2	CC7A
(TOTLZ=0161)	
U 72- 3	7524
U 72- 4	HHCH
U 72- 5	A899
U 72- 6	7524
U 72- 7	CC7A
U 72- 9	high
U 72-10	high
U 72-12	high
U 72-13	A899
U 72-14	CC7A
(TOTLZ=0161)	
U 72-15	CC7A
(TOTLZ=0391)	
U 73- 1	13P3
U 73- 2	A899
U 73- 3	CC7A
(TOTLZ=0161)	
U 73- 4	0000

```
U 73- 5  CC7A
(TOTLZ=0161)
U 73- 6  CC7A
U 73- 8  7524
U 73- 9  CC7A
(TOTLZ=0161)
U 73-10  FP5P
U 73-11  CC7A
(TOTLZ=2187)
U 73-12  HHCH
U 73-13  0000
(TOTLZ=0001)
U 75- 1  CC7A
(TOTLZ=1195)
U 75- 2  CC7A
(TOTLZ=0161)
U 75- 3  high
U 75- 4  CC7A
(TOTLZ=0161)
U 75- 5  CC7A
(TOTLZ=2187)
U 75- 6  CC7A
(TOTLZ=0161)
U 75- 8  high
U 75- 9  CC7A
(TOTLZ=0161)
U 75-10  high
U 75-11  CC7A
(TOTLZ=0161)
U 75-12  0000
(TOTLZ=0161)
U 75-13  CC7A
(TOTLZ=2187)
U 81- 2  7524
U 81- 3  HHCH
U 81- 4  13P3
U 81- 5  high
U 81- 6  A899
U 81-10  high
U 81-11  low
U 81-12  high
U 81-13  high
U 82- 1  A899
U 82- 4  9UA5
U 82- 5  7F14
U 82- 6  8808
U 82- 7  487C
U 82- 9  870C
U 82-10  low
U 82-12  high
U 82-13  870C
U 82-14  high
U 82-15  high
```

64602A Timing Acquisition Board
RAM COUNTERS #2

NORM MODE VH = UP73

DATA THRESHOLD : ecl & ttl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: sa gate neg. edge
Location of QUAL/STOP: sa gate pos. edge
Location of CLOCK: sa clk pos. edge
Location of GROUND: gnd

ECL

U 5- 3	0402	
U 5- 7	0200	
U 5-11	U5U6	
U 5-15	U3U4	
U 6- 1	high	
U 6- 2	U3U4	
U 6- 3	0402	
U 6- 4	U1U4	
U 6- 5	high	
U 6- 6	U5U6	
U 6- 7	0U87	
U 6-10	U3U4	
U 6-11	0U87	
U 6-12	high	
U 6-13	U1U4	
U 6-15	U5U6	
U 7- 2	0985	
U 7- 4	U7U6	
U 7- 5	0985	
U 7- 9	0000	
U 7-10	U7U6	
U 7-11	0985	
U 7-14	0985	
U 9- 1	high	
U 9- 2	U7U6	
U 9- 3	U7U6	
U 9- 4	low	
U 9- 5	0985	
U 10- 2	U1U4	
U 10- 3	0U87	
U 10- 4	U1U4	
U 10- 5	0U87	
U 10- 6	0985	
U 10- 7	U7U6	
U 10- 9	0000	
U 10-10	U7U6	
U 10-13	U7U6	
U 10-14	0985	
U 10-15	U7U6	
U 14- 1	high	
U 14- 2	A1H8	
U 14- 3	high	
U 14- 4	A1H8	
U 14- 6	5UAC	
U 14- 7	UP73	
U 14- 9	5UAC	
U 14-10	A1H8	
U 14-12	UP73	
(TOTLZ=0001)		
U 14-13	0000	
U 14-14	high	
U 14-15	0U87	
U 16- 3	40A5	
U 16- 6	40A5	
U 22- 6	U3U4	
U 22-14	U5U6	

TTL

U 4- 1	0200	
U 4- 2	U1U4	
U 4- 3	0F06	
U 4- 4	high	
U 4- 5	0U87	
U 4- 6	U1U4	
U 4- 7	UUU3	
U 4- 9	0180	
U 4-10	high	
U 4-11	0UP6	
U 4-12	UUU3	
U 4-13	0200	
U 4-14	0U87	
U 4-15	CPH6	
U 5- 4	0402	
U 5-12	U5U6	
U 5-13	U3U4	
U 16- 4	40A5	
U 16- 5	CPH6	
U 22- 7	40A5	
U 22-15	741F	
U 23- 7	40A5	
U 23-15	741F	
U 24- 7	40A5	
U 24-15	8A6U	
U 25- 7	40A5	
U 25-15	8A6U	
U 29- 7	40A5	

```
U 65- 3  0040
U 65- 4  2052
U 65- 5  0040
U 65- 6  2052
U 65- 7  5UAC
U 65- 9  5UAC
U 65-10  0804
U 65-11  387U
U 65-12  0864
U 65-13  387U
U 65-14  0864
U 65-15  0804
U 66- 1  CPH6
U 66- 2  0200
U 66- 3  0040
U 66- 4  2052
U 66- 5  0040
U 66- 6  2052
U 66- 7  5UAC
U 66- 9  5UAC
U 66-10  0F06
U 66-11  3F7H
U 66-12  0F66
U 66-13  3F7H
U 66-14  0F66
U 66-15  0F06
U 67- 1  low
U 67- 2  UP33
U 67- 3  0040
U 67- 4  HP21
U 67- 5  2052
U 67- 6  UP33
U 67- 7  0040
U 67- 8  HP21
U 67- 9  2052
U 67-11  HP21
U 67-12  2052
U 67-13  UP33
U 67-14  0040
U 67-15  HP21
U 67-16  2052
U 67-17  UP33
U 67-18  0040
U 67-19  low
U 68- 1  CPH6
U 68- 2  0402
U 68- 3  0040
U 68- 4  2052
U 68- 5  0040
U 68- 6  2052
U 68- 7  5UAC
U 68- 9  5UAC
U 68-10  high
U 68-11  387U
U 68-12  0864
U 68-13  387P
U 68-14  0CP4
U 68-15  0804
U 69- 1  CPH6
U 69- 2  0200
U 69- 3  0040
U 69- 4  2052
U 69- 5  0040
U 69- 6  2052
U 69- 7  5UAC
U 69- 9  5UAC
U 69-10  high
U 69-11  3F7H
U 69-12  0F66
U 69-13  3F7F
U 69-14  0UP6
U 69-15  0F06
U 70- 1  low
U 70- 4  5UAC
U 70- 5  7U39
U 70- 6  UP73
(TOTLZ=0001)
U 70- 7  2192
U 70- 8  741F
U 70- 9  7U38
U 70-11  high
U 70-12  741F
U 70-13  0180
U 70-14  0000
(TOTLZ=0001)
U 70-15  high
U 70-16  5UAC
U 70-17  0000
U 70-18  0000
U 70-19  A1H8
U 72- 1  high
U 72- 2  UP73
(TOTLZ=0001)
U 72- 3  UP73
(TOTLZ=0091)
U 72- 4  5UAC
U 72- 5  A1H8
U 72- 6  high
U 72- 7  high
U 72- 9  high
U 72-10  high
U 72-11  high
U 72-12  high
U 72-13  A1H8
U 72-14  UP73
(TOTLZ=0001)
U 72-15  UP73
(TOTLZ=0123)
U 73- 1  5UAC
U 73- 2  A1H8
U 73- 3  UP73
(TOTLZ=0001)
U 73- 4  low
U 73- 5  UP73
(TOTLZ=0001)
U 73- 6  high
U 73- 8  high
U 73- 9  UP73
(TOTLZ=0001)
U 73-10  low
U 73-11  UP73
(TOTLZ=0199)
U 73-12  5UAC
U 79- 1  A1H8
U 79- 2  0864
U 79- 3  6715
U 79- 4  387U
U 79- 5  771H
U 79- 6  0864
U 79- 7  6794
U 79- 8  387U
U 79- 9  741F
U 79-11  0CP4
U 79-12  6715
U 79-13  387P
U 79-14  771H
U 79-15  0864
U 79-16  6715
U 79-17  387U
U 79-18  771H
U 79-19  A1H8
U 81- 4  5UAC
U 81- 5  high
U 81- 6  A1H8
U 81- 8  8A6U
U 81- 9  741F
U 81-10  high
U 82- 1  A1H8
U 82- 2  0UP6
U 82- 3  701P
U 82- 4  low
U 82- 5  7U39
U 82- 6  high
U 82- 7  2093
U 82- 9  7U38
U 82-10  low
U 82-11  771H
U 82-12  high
U 82-13  7U39
U 82-14  high
U 82-15  high
```

64602A Timing Acquisition Board
FAST SAMPLE #3

NORM MODE VH = FH25

DATA THRESHOLD: ecl & ttl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: sa gate neg. edge
Location of QUAL/STOP: sa gate pos. edge
Location of CLOCK: sa clk pos. edge
Location of GROUND: gnd

ECL

U 7- 1	high	U 12- 3	F070	U 27-18	5852
U 7- 2	0000	U 12- 4	F070	U 27-19	5852
U 7- 4	3395	U 12-14	6692	U 27-20	9577
U 7- 5	0000	U 14- 1	high	U 27-21	5852
U 7-11	0000	U 14- 2	ACC7	U 27-22	5852
U 7-12	A755	U 14- 3	FH25	U 27-23	9577
U 7-13	6A70	U 14- 4	ACC7	U 27-24	5852
U 7-14	0000	U 14- 5	6692	U 27-25	5852
U 7-15	A755	U 14- 6	6692	U 27-26	9577
U 9- 1	high	U 14- 7	FH25	U 27-28	high
U 9- 2	3395	U 14- 9	6692	U 27-29	3395
U 9- 3	3395	U 14-10	ACC7	U 27-31	AF8C
U 9- 4	low	U 14-11	high	U 27-32	high
U 9- 5	0000	U 14-12	FH25	U 27-33	low
U 9- 6	high	U 14-14	high	U 27-34	high
U 9- 7	0000	U 14-15	677P	U 27-35	3PF0
U 9-10	0000	U 16- 3	0000	U 27-36	U3P5
U 9-11	0H55	U 16- 6	0000	U 27-37	5H96
U 9-12	0000	U 16-11	9998	U 27-38	3PF0
U 9-13	F070	U 16-15	U836	U 27-39	U3P5
U 9-14	3395	U 17- 2	9998	U 27-40	5H96
U 9-15	3395	U 17- 3	AF8C		
U 10- 1	high	U 17- 5	U836		
U 10- 2	AA5C	U 27- 1	3PF0		
U 10- 3	677P	U 27- 2	U3P5		
U 10- 4	AA5C	U 27- 3	5H96		
U 10- 5	677P	U 27- 4	9577		
U 10- 6	0000	U 27- 5	5852		
U 10- 7	3395	U 27- 6	U621		
U 10- 9	0000	U 27- 8	U836		
U 10-10	3395	U 27- 9	high		
U 10-11	0000	U 27-10	A755		
U 10-12	0000	U 27-12	3395		
U 10-13	3395	U 27-13	high		
U 10-14	0000	U 27-14	3395		
U 10-15	3395	U 27-15	5852		
U 11-13	6A70	U 27-16	5852		
U 12- 2	0H55	U 27-17	9577		

TTL

U 4- 2	AA5C	U 72- 4	6692	U 82- 6	U836
U 4- 3	0000	U 72- 5	18F5	U 82- 7	322H
(TOTLZ=0015)		U 72- 6	6A70	U 82- 9	322H
U 4- 4	high	U 72- 7	H902	U 82-10	low
U 4- 5	677P	U 72- 9	4F41	U 82-12	high
U 4- 6	AA5C	U 72-10	1946	U 82-13	P7FA
U 4- 7	AA5C	U 72-11	high	U 82-14	high
U 4- 9	677P	U 72-12	high	U 82-15	high
U 4-10	high	U 72-13	0FP2		
U 4-12	AA5C	U 72-14	FH25		
U 4-14	677P	U 72-15	9822		
U 4-15	FH25	U 73- 1	H5P0		
U 11- 7	C18H	U 73- 2	18F5		
U 11-11	A755	U 73- 3	FH25		
U 12- 5	0H55	U 73- 4	1427		
U 12- 7	4HF5	U 73- 5	FH25		
U 12-11	6692	U 73- 6	H902		
U 16- 4	0000	U 73- 8	6A70		
U 16- 5	FH25	U 73- 9	FH25		
U 16-12	9998	U 73-10	A755		
U 16-13	U836	U 73-11	FH25		
U 70- 1	low	U 73-12	6692		
U 70- 4	6692	U 73-13	0000		
U 70- 5	P7FA	U 75- 1	FH25		
U 70- 6	FH25	(TOTLZ=0059)			
U 70- 7	681A	U 75- 2	FH25		
U 70- 8	C18H	U 75- 3	high		
U 70- 9	4782	U 75- 4	FH25		
U 70-11	4HF5	U 75- 5	FH25		
U 70-12	C18H	(TOTLZ=0207)			
U 70-13	677P	U 75- 6	FH25		
U 70-14	0000	U 75- 8	high		
U 70-15	0H55	U 75- 9	FH25		
U 70-16	6692	U 75-10	high		
U 70-19	18F5	U 75-11	FH25		
U 71- 1	high	U 75-12	0000		
U 71- 2	4F41	U 75-13	FH25		
U 71- 3	4F41	(TOTLZ=0207)			
U 71- 4	1427	U 81- 2	7P57		
U 71- 5	high	U 81- 3	6692		
U 71- 6	4HF5	U 81- 4	H5P0		
U 71- 7	80P0	U 81- 5	high		
U 71- 9	F070	U 81- 6	18F5		
U 71-10	0H55	U 81- 9	C18H		
U 71-11	high	U 81-10	high		
U 71-12	A755	U 81-11	low		
U 71-13	1946	U 81-12	high		
U 71-14	1946	U 81-13	high		
U 71-15	high	U 82- 1	18F5		
U 72- 1	high	U 82- 3	322H		
U 72- 2	FH25	U 82- 4	9998		
U 72- 3	7P57	U 82- 5	P7FH		

64602A Timing Acquisition Board
DUAL THRESHOLD #4

NORM MODE VH = 75CC

DATA THRESHOLD: ecl & ttl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: sa gate neg. edge
Location of QUAL/STOP: sa gate pos. edge
Location of CLOCK: sa clk pos. edge
Location of GROUND: gnd

ECL

U 7-13	1H46
U 7-15	68UH
U 11- 3	7P00
U 11-13	1H46
U 12- 3	6PCP
U 12-14	3AHH
U 16-11	442A
U 16-15	54A6
U 17- 2	442A
U 17- 3	6537
U 17- 5	54A6
U 27- 1	H2CF
U 27- 2	A707
U 27- 3	low
U 27- 4	H2CF
U 27- 5	A707
U 27- 6	low
U 27- 7	7P00
U 27- 8	54A6
U 27- 9	high
U 27-10	68UH
U 27-11	low
U 27-12	high
U 27-13	high
U 27-14	high
U 27-15	low
U 27-16	6FAP
U 27-17	1915
U 27-18	low
U 27-19	6FAP
U 27-20	1915
U 27-21	low
U 27-22	6FAP
U 27-23	1915
U 27-24	low
U 27-25	6FAP
U 27-26	1915
U 27-27	high
U 27-28	high
U 27-29	high
U 27-30	low
U 27-31	6537
U 27-32	high
U 27-33	low
U 27-34	high
U 27-35	H2CF
U 27-36	A707
U 27-37	low
U 27-38	H2CF
U 27-39	A707
U 27-40	low

TTL

U 11- 7	0CCC
U 11-11	68UH
U 12- 7	A8F7
U 12-11	3AHH
U 16-12	442A
U 16-13	54A6
U 22-15	0CCC
U 23-15	0CCC
U 24-15	7P00
U 25-15	7P00
U 29-15	7P00
U 30-15	7P00
U 31-15	0CCC
U 32-15	0CCC
U 70- 1	low
U 70- 4	3AHH
U 70- 5	8580
U 70- 6	75CC
U 70- 7	545U
U 70- 8	0CCC
U 70- 9	8FCU
U 70-11	A8F7
U 70-12	0CCC
U 70-13	low
U 70-14	0000
U 70-15	high
U 70-16	3AHH
U 70-19	HP3P
U 71- 1	high
U 71- 2	P4A6
U 71- 3	P4A6
U 71- 4	U9A5
U 71- 5	high
U 71- 6	A8F7
U 71- 7	HH7F
U 71- 9	low
U 71-10	high
U 71-11	high

```
U 71-12  68UH
U 71-13  high
U 71-14  high
U 71-15  high
U 72- 1  high
U 72- 2  75CC
U 72- 3  P4P3
U 72- 4  3AHH
U 72- 5  HP3P
U 72- 6  1H46
U 72- 7  8F1P
U 72- 9  P4A6
U 72-10  high
U 72-11  high
U 72-12  high
U 72-13  279C
U 72-14  75CC
U 72-15  P4A6
U 73- 1  AC85
U 73- 2  HP3P
U 73- 3  75CC
U 73- 4  U9A5
U 73- 5  75CC
U 73- 6  8F1P
U 73- 8  1H46
U 73- 9  75CC
U 73-10  68UH
U 73-11  75CC
(TOTLZ=0207)
U 73-12  3AHH
U 73-13  0000
U 76- 2  U48A
U 76- 3  5125
U 76- 4  A2HA
U 76- 5  UPH0
U 76- 6  0H2U
U 76- 7  5125
U 76- 8  U1UF
U 76- 9  0CCC
U 76-11  8F1P
U 76-13  75CC
U 76-19  1367
U 78- 2  650H
U 78- 3  545U
U 78- 4  8FCU
U 78- 5  8580
U 78- 6  767U
U 78- 7  6794
U 78- 8  H98A
U 78- 9  8580
U 78-11  8F1P
U 78-13  75CC
U 78-19  8U27
U 81- 2  P4P3
U 81- 3  3AHH
U 81- 4  AC85
U 81- 5  high
U 81- 6  HP3P
U 81- 8  7P00
U 81- 9  0CCC
U 81-10  high
U 81-11  low
U 81-12  high
U 81-13  high
U 82- 1  HP3P
U 82- 2  low
U 82- 3  8580
U 82- 4  442A
U 82- 5  6794
U 82- 6  54A6
U 82- 7  H98A
U 82- 9  767U
U 82-10  low
U 82-11  5125
U 82-12  high
U 82-13  8580
U 82-14  high
U 82-15  high
```

64602A Timing Acquisition Board
GLITCH #5

NORM MODE VH = 75UA

DATA THRESHOLD HIGH: ecl & ttl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: sa gate neg. edge
Location of QUAL/STOP: sa gate pos. edge
Location of CLOCK: sa clk pos. edge
Location of GROUND: gnd

ECL

U	5- 3	41P2	U	9-14	796U	U	22-14	41P2
U	5- 7	3C6F	U	9-15	796U	U	22-35	796U
U	5-11	41P2	U	10- 1	high	U	23-35	796U
U	5-15	3C6F	U	10- 2	0000	U	24-35	796U
U	6- 1	high	U	10- 3	75UA	U	25-35	796U
U	6- 2	3C6F	U	10- 4	0000	U	27- 1	4CF6
U	6- 3	41P2	U	10- 5	75UA	U	27- 2	3P3F
U	6- 4	0000	U	10- 6	0F95	U	27- 3	0000
U	6- 5	high	U	10- 7	796U	U	27- 4	4CF6
U	6- 6	41P2	U	10- 9	0000	U	27- 5	3P3F
U	6- 7	75UA	U	10-10	796U	U	27- 6	0000
U	6-10	3C6F	U	10-11	0000	U	27- 7	8A13
U	6-11	75UA	U	10-12	0000	U	27- 8	3C3F
U	6-12	high	U	10-13	796U	U	27- 9	high
U	6-13	0000	U	10-14	0F95	U	27-10	8H66
U	6-14	3C6F	U	10-15	796U	U	27-11	0F95
U	6-15	41P2	U	11- 3	8A13	U	27-12	796U
U	7- 1	high	U	11-13	U89F	U	27-13	high
U	7- 2	0F95	U	12- 3	0669	U	27-14	796U
U	7- 3	0000	U	12-14	CAUH	U	27-15	18CP
U	7- 4	796U	U	14- 1	high	U	27-16	3P3F
U	7- 5	0F95	U	14- 2	FU07	U	27-17	4CF6
U	7-10	796U	U	14- 3	75UA	U	27-18	18CP
U	7-11	0F95	U	14- 4	FU07	U	27-19	3P3F
U	7-12	8H66	U	14- 5	CAUH	U	27-20	4CF6
U	7-13	U89F	U	14- 6	CAUH	U	27-21	18CP
U	7-14	0F95	U	14- 7	75UA	U	27-22	3P3F
U	7-15	8H66	U	14- 9	CAUH	U	27-23	4CF6
U	9- 1	high	U	14-10	FU07	U	27-24	18CP
U	9- 2	796U	U	14-12	75UA	U	27-25	3P3F
U	9- 3	796U	U	14-14	high	U	27-26	4CF6
U	9- 5	0F95	U	14-15	75UA	U	27-27	796U
U	9- 6	high	U	16-11	73H5	U	27-28	high
U	9- 7	0F95	U	16-15	3C3F	U	27-29	796U
U	9-10	0F95	U	17- 2	73H5	U	27-30	0F95
U	9-11	high	U	17- 3	3H13	U	27-31	3H13
U	9-12	0F95	U	17- 5	3C3F	U	27-32	high
U	9-13	low	U	22- 6	3C6F	U	27-33	low

U 27-34	high
U 27-35	4CF6
U 27-36	3P3F
U 27-37	0000
U 27-38	4CF6
U 27-39	3P3F
U 27-40	0000
U 29-35	796U
U 30-35	796U
U 31-35	796U
U 32-35	796U

TTL

U 5- 4	41P2
U 5- 5	3C6F
U 5-12	41P2
U 5-13	3C6F
U 11- 7	UUP9
U 11-11	8H66
U 12- 7	P727
U 12-11	CAUH
U 16-12	73H5
U 16-13	3C3F
U 22- 1	F07H
U 22- 2	436C
U 22- 3	low
U 22- 4	low
U 22-15	UUP9
U 22-17	low
U 22-18	low
U 22-19	low
U 22-20	low
U 22-21	low
U 22-22	5436
U 22-23	6P48
U 22-24	low
U 22-37	low
U 22-38	00U9
U 22-39	low
U 22-40	4373
U 23- 1	CPC2
U 23- 2	CPC2
U 23- 3	374A
U 23- 4	374A
U 23-15	UUP9
U 23-17	74PU
U 23-18	74PU
U 23-19	74PU
U 23-20	74PU
U 23-21	4FH6
U 23-22	2C0A
U 23-23	45A3
U 23-24	45A3
U 23-37	PF12
U 23-38	PF12
U 23-39	65PA
U 23-40	65PA
U 24- 1	F07H
U 24- 2	436C
U 24- 3	low
U 24- 4	low
U 24-15	8A13
U 24-17	low
U 24-18	low
U 24-19	low
U 24-20	low
U 24-21	low
U 24-22	5436
U 24-23	6P48
U 24-24	low
U 24-37	low
U 24-38	00U9
U 24-39	low
U 24-40	4373
U 25- 1	CPC2
U 25- 2	CPC2
U 25- 3	374A
U 25- 4	374A
U 25-15	8A13
U 25-17	74PU
U 25-18	74PU
U 25-19	74PU
U 25-20	74PU
U 25-21	4FH6
U 25-22	2C0A
U 25-23	45A3
U 25-24	45A3
U 25-37	PF12
U 25-38	PF12
U 25-39	65PA
U 25-40	65PA
U 29- 1	F07H
U 29- 2	436C
U 29- 3	low
U 29- 4	low
U 29-15	8A13
U 29-17	low
U 29-18	low
U 29-19	low
U 29-20	low
U 29-21	low
U 29-22	5436
U 29-23	6P48
U 29-24	low
U 29-37	low
U 29-38	00U9
U 29-39	low
U 29-40	4373
U 30- 1	CPC2
U 30- 2	CPC2
U 30- 3	374A
U 30- 4	374A
U 30-15	8A13
U 30-17	74PU
U 30-18	74PU
U 30-19	74PU
U 30-20	74PU

U 30-21 4FH6
U 30-22 2C0A
U 30-23 45A3
U 30-24 45A3
U 30-37 PF12
U 30-38 PF12
U 30-39 65PA
U 30-40 65PA
U 31- 1 F07H
U 31- 2 436C
U 31- 3 low
U 31- 4 low
U 31-15 UUP9
U 31-17 low
U 31-18 low
U 31-19 low
U 31-20 low
U 31-21 low
U 31-22 5436
U 31-23 6P48
U 31-24 low
U 31-37 low
U 31-38 00U9
U 31-39 low
U 31-40 4373
U 32- 1 CPC2
U 32- 2 CPC2
U 32- 3 374A
U 32- 4 374A
U 32-15 UUP9
U 32-17 74PU
U 32-18 74PU
U 32-19 74PU
U 32-20 74PU
U 32-21 4FH6
U 32-22 2C0A
U 32-23 45A3
U 32-24 45A3
U 32-37 PF12
U 32-38 PF12
U 32-39 65PA
U 32-40 65PA
U 70- 1 low
U 70- 2 75UA
U 70- 4 CAUH
U 70- 5 H3P8
U 70- 6 75UA
U 70- 7 U251
U 70- 8 UUP9
U 70- 9 3267
U 70-11 P727
U 70-12 UUP9
U 70-13 low
U 70-14 0000
U 70-15 high
U 70-16 CAUH
U 70-19 high
U 71- 1 high
U 71- 2 A546
U 71- 3 A546
U 71- 4 379C
U 71- 5 high
U 71- 6 P727
U 72- 1 high
U 72- 2 75UA
U 72- 3 FU07
U 72- 4 CAUH
U 72- 5 high
U 72- 6 U89F
U 72- 7 4261
U 72- 9 A546
U 72-10 high
U 72-11 high
U 72-12 high
U 72-13 4261
U 72-14 75UA
U 72-15 A546
U 73- 1 low
U 73- 2 high
U 73- 3 75UA
U 73- 4 379C
U 73- 5 75UA
U 73- 6 4261
U 73- 8 U89F
U 73- 9 75UA
U 73-10 8H66
U 73-11 75UA
(TOTLZ=0207)
U 73-12 CAUH
U 73-13 0000
U 76- 2 4H23
U 76- 3 7HAU
U 76- 4 2H9C
U 76- 5 H3P8
U 76- 6 7AC8
U 76- 7 HP50
U 76- 8 6A64
U 76- 9 UUP9
U 76-11 4261
U 76-13 75UA
U 76-19 4CF6
U 78- 2 1520
U 78- 3 U251
U 78- 4 3267
U 78- 5 H3P8
U 78- 6 7AC8
U 78- 7 7HAU
U 78- 8 2H9C
U 78- 9 H3P8
U 78-11 4261
U 78-13 75UA
U 78-19 4CF6

64602A Timing Acquisition Board
DACS TRIGGER #6

NORM MODE VH = H7CH

DATA THRESHOLD: ecl & ttl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: sa gate neg. edge
Location of QUAL/STOP: sa gate pos. edge
Location of CLOCK: sa clock pos. edge
Location of GROUND: gnd

ECL

U 7-12	2619
U 7-13	U1A4
U 7-15	2619
U 11-13	U1A4
U 12-14	PCHP
U 16-11	CC3A
U 16-15	A24P
U 17- 2	CC3A
U 17- 3	FPF9
U 17- 5	A24P
U 22-26	P620
U 23-26	7309
U 24-26	P620
U 25-26	7309
U 27- 1	623C
U 27- 2	C586
U 27- 3	P620
U 27- 4	623C
U 27- 5	C586
U 27- 6	P620
U 27- 8	A24P
U 27- 9	high
U 27-10	2619
U 27-13	high
U 27-15	7309
U 27-16	724H
U 27-17	A5U0
U 27-18	7309
U 27-19	724H
U 27-20	A5U0
U 27-21	7309
U 27-22	724H
U 27-23	A5U0
U 27-24	7309
U 27-25	724H
U 27-26	A5U0
U 27-28	high
U 27-31	FPF9
U 27-32	high
U 27-33	low
U 27-34	high
U 27-35	623C
U 27-36	C586
U 27-37	P620
U 27-38	623C
U 27-39	C586
U 27-40	P620
U 29-26	P620
U 30-26	7309
U 31-26	P620
U 32-26	7309

TTL

U 11-11	2619
U 12-11	PCHP
U 16-12	CC3A
U 16-13	A24P
U 70- 1	low
U 70- 4	PCHP
U 70- 5	CHF1
U 70- 6	H7CH
U 70- 7	HA87
U 70- 9	1P78
U 70-11	high
U 70-13	73F7
U 70-14	0000
U 70-15	high
U 70-16	PCHP
U 70-19	P711
U 72- 1	high
U 72- 2	H7CH
U 72- 3	0FFU
U 72- 4	PCHP
U 72- 5	P711
U 72- 6	U1A4
U 72- 7	2AH6
U 72- 9	high
U 72-10	high
U 72-11	high
U 72-12	high
U 72-13	1A7A
U 72-14	H7CH
U 72-15	H7CH
(TOTLZ=0125)	
U 73- 1	30AF
U 73- 2	P711
U 73- 3	H7CH
U 73- 4	UH6C
U 73- 5	H7CH
U 73- 6	2AH6
U 73- 8	U1A4

```
U 73- 9  H7CH
U 73-10  2619
U 73-11  H7CH
(TOTLZ=0207)
U 73-12  PCHP
U 73-13  0000
U 76- 2  P2U0
U 76-10  low
U 76-11  2AH6
U 76-13  H7CH
U 76-19  FFAC
U 78- 2  3P15
U 78- 3  HA87
U 78- 4  1P78
U 78- 5  CHF1
U 78- 6  U401
U 78- 7  3801
U 78- 8  U311
U 78-10  low
U 78-11  2AH6
U 78-13  H7CH
U 78-19  F47A
U 81- 2  0FFU
U 81- 3  PCHP
U 81- 4  30AF
U 81- 5  high
U 81- 6  P711
U 81-10  high
U 81-11  low
U 81-12  high
U 81-13  high
U 82- 1  P711
U 82- 4  CC3A
U 82- 5  3801
U 82- 6  A24P
U 82- 7  U311
U 82- 9  U401
U 82-10  low
U 82-12  high
U 82-13  CHF1
U 82-14  high
U 82-15  high
```

64602A Timing Acquisition Board
CHECKER BOARD #7

NORM MODE VH = UF19

[redacted]

CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: sa gate neg. edge
Location of QUAL/STOP: sa gate pos. edge
Location of CLOCK: sa clk pos. edge
Location of GROUND: gnd

ECL

U	5-11	0000
U	5-15	F1CU
U	11- 3	6P32
U	11-12	F1CU
U	12-15	F1CU
U	22- 6	F1CU
U	22-14	F1CU

TTL

U	5-12	F1CU
U	5-13	F1CU
U	11- 7	922C
U	11-10	UF19
(TOTLZ=4625)		
U	12-10	F1CU
U	22 1	7PH1
	2	82F8
U	23 3	7PH1
	4	82F8
U	31 12	3HA6
	15	922C
U	32 17	U026
	18	FH80
	19	U026
	20	FH80
	21	U026
	22	FH80
	23	U026
	24	FH80
	37	7PH1
	38	82F8
	39	7PH1
	40	82F8
U	24 1	82F8
	2	7PH1
U	25 3	82F8
	4	7PH1
U	29 12	3HA6
	22	U026
	23	FH80
	24	U026
	37	82F8
	38	7PH1
	39	82F8
	40	7PH1
U	33 1	7450
	2	315C
U	34 3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	82F8
	10	5684
	11	7PH1
	12	AA9H
	13	82F8
	14	5684
	15	7PH1
	16	AA9H
	17	high
	18	A7CU
	19	low
	20	F1CU
	21	1561
	22	high
U	35 1	7450

	8	low
	9	82F8
	10	5684
	11	7PH1
	12	AA9H
	13	82F8
	14	5684
	15	7PH1
	16	AA9H
	17	high
	18	PCUF
	19	low
	20	F1CU
	21	1561
	22	high
U 37	1	7450
|	2	315C
U 38	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	7PH1
	10	5684
	11	82F8
	12	AA9H
	13	7PH1
	14	5684
	15	82F8
	16	AA9H
	17	high
	18	7318
	19	low
	20	F1CU
	21	1561
	22	high
U 39	1	7450
|	2	315C
U 40	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	7PH1
	10	5684
	11	82F8
	12	AA9H
	13	7PH1
	14	5684
	15	82F8
	16	AA9H
	17	high
	18	7F28
	19	low
	20	F1CU
	21	1561
	22	high
U 41	1	7450
|	2	315C
U 42	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	7PH1
	10	5684
	11	82F8
	12	AA9H
	13	7PH1
	14	5684
	15	82F8
	16	AA9H
	17	high
	18	4076
	19	low
	20	F1CU
	21	1561
	22	high
U 43	1	7450
|	2	315C
U 44	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	7PH1
	10	5684
	11	82F8
	12	AA9H
	13	7PH1
	14	5684
	15	82F8
	16	AA9H
	17	high
	18	577U
	19	low
	20	F1CU
	21	1561
	22	high
U 45	1	7450
|	2	315C
U 46	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	7PH1
	10	5684
	11	7PH1
	12	AA9H
	13	82F8
	14	5684
	15	7PH1
	16	AA9H
	17	high
	18	P721
	19	low
	20	F1CU
	21	1561
	22	high
U 47	1	7450
|	2	315C
U 48	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	82F8
	10	5684
	11	7PH1
	12	AA9H
	13	82F8
	14	5684
	15	7PH1
	16	AA9H
	17	high
	18	A800
	19	low
	20	F1CU
	21	1561
	22	high
U 49	1	7450
|	2	315C
U 50	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	U026
	10	C65H
	11	FH80
	12	AA9H

	13	U026
	14	C65H
	15	FH80
	16	AA9H
	17	high
	18	A7CU
	19	low
	20	F1CU
	21	1561
	22	high
U 51	1	7450
|	2	315C
U 52	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	U026
	10	C65H
	11	FH80
	12	AA9H
	13	U026
	14	C65H
	15	FH80
	16	AA9H
	17	high
	18	PCUF
	19	low
	20	F1CU
	21	1561
	22	high
U 53	1	7450
|	2	315C
U 54	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	FH80
	10	C65H
	11	U026
	12	AA9H
	13	FH80
	14	C65H
	15	U026
	16	AA9H
	17	high
	18	7318
	19	low
	20	F1CU
	21	1561
	22	high
U 55	1	7450
|	2	315C
U 56	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	FH80
	10	C65H
	11	U026
	12	AA9H
	13	FH80
	14	C65H
	15	U026
	16	AA9H
	17	high
	18	7F28
	19	low
	20	F1CU
	21	1561
	22	high
U 57	1	7450
|	2	315C
U 58	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	FH80
	10	C65H
	11	U026
	12	AA9H
	13	FH80
	14	C65H
	15	U026
	16	AA9H
	17	high
	18	4076
	19	low
	20	F1CU
	21	1561
	22	high
U 59	1	7450
|	2	315C
U 60	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	FH80
	10	C65H
	11	U026
	12	AA9H
	13	FH80
	14	C65H
	15	U026
	16	AA9H
	17	high
	18	577U
	19	low
	20	F1CU
	21	1561
	22	high
U 61	1	7450
|	2	315C
U 62	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	U026
	10	C65H
	11	FH80
	12	AA9H
	13	U026
	14	C65H
	15	FH80
	16	AA9H
	17	high
	18	P721
	19	low
	20	F1CU
	21	1561
	22	high
U 63	1	7450
|	2	315C
U 64	3	U437
	4	1F58
	5	U9AF
	6	2702
	7	705A
	8	low
	9	U026
	10	C65H
	11	FH80
	12	AA9H
	13	U026
	14	C65H
	15	FH80
	16	AA9H
	17	high

```
      18  A800
      19  low
      20  F1CU
      21  1561
      22  high
U 65- 1  UF19
(TOTLZ=0002)
U 65- 2  0000
(TOTLZ=4625)
U 65- 3  1561
U 65- 4  U9AF
U 65- 5  2702
U 65- 6  705A
U 65- 7  0000
(TOTLZ=4625)
U 65- 9  0000
(TOTLZ= 4625)
U 65-10  3UA3
U 65-11  705A
U 65-12  2702
U 65-13  U9AF
U 65-14  1561
U 65-15  4CF9
U 66- 1  UF19
(TOTLZ=0002)
U 66- 2  0000
(TOTLZ=4625)
U 66- 3  1561
U 66- 4  U9AF
U 66- 5  2702
U 66- 6  705A
U 66- 7  0000
(TOTLZ=4625)
U 66- 9  0000
(TOTLZ= 4625)
U 66-10  3UA3
U 66-11  705A
U 66-12  2702
U 66-13  U9AF
U 66-14  1561
U 66-15  4CF9
U 67- 1  low
U 67- 2  P041
U 67- 3  1561
U 67- 4  082P
U 67- 5  U9AF
U 67- 6  FH42
U 67- 7  2702
U 67- 8  8849
U 67- 9  705A
U 67-11  8F43
U 67-12  7450
U 67-13  HC1C
U 67-14  315C
U 67-15  05C5
U 67-16  U437
U 67-17  P978
U 67-18  1F58
U 67-19  low
U 68- 1  UF19
(TOTLZ=0002)
U 68- 2  0000
(TOTLZ=4625)
U 68- 3  1F58
U 68- 4  U437
U 68- 5  315C
U 68- 6  7450
U 68- 7  0000
(TOTLZ=4625)
U 68- 9  0000
(TOTLZ=4625)
U 68-10  high
U 68-11  7450
U 68-12  315C
U 68-13  U437
U 68-14  1F58
U 68-15  3UA3
U 69- 1  UF19
(TOTLZ=0002)
U 69- 2  0000
(TOTLZ=4625)
U 69- 3  1F58
U 69- 4  U437
U 69- 5  315C
U 69- 6  7450
U 69- 7  0000
(TOTLZ=4625)
U 69- 9  0000
(TOTLZ=4625)
U 69-10  high
U 69-11  7450
U 69-12  315C
U 69-13  U437
U 69-14  1F58
U 69-15  3UA3
U 70- 1  low
U 70- 4  0000
(TOTLZ=4625)
U 70- 5  FH6H
U 70- 6  UF19
(TOTLZ=4625)
U 70- 7  H636
U 70- 8  922C
U 70- 9  FH6H
U 70-11  high
U 70-12  922C
U 70-13  727U
U 70-14  0000
(TOTLZ=4625)
U 70-15  high
U 70-16  0000
U 70-19  high
U 72- 1  high
U 72- 2  UF19
(TOTLZ=4625)
U 72- 3  UF19
(TOTLZ=0FLO)
U 72- 4  0000
(TOTLZ=4625)
U 72- 5  high
U 72- 6  high
U 72- 7  high
U 72- 9  high
U 72-10  high
U 72-12  F1CU
U 72-13  UF19
(TOTLZ=49743)
U 72-14  UF19
(TOTLZ=4625)
U 72-15  F1CU
U 73- 1  low
U 73- 2  high
U 73- 3  UF19
(TOTLZ=4625)
U 73- 4  low
U 73- 5  UF19
(TOTLZ=4625)
U 73- 6  high
U 73- 8  high
U 73- 9  UF19
(TOTLZ=4625)
U 73-10  low
U 73-11  UF19
(TOTLZ=0FLO)
U 73-12  0000
U 73-13  UF19
(TOTLZ=4625)
U 74- 1  922C
U 74- 2  A9F0
U 74- 3  PHA9
U 74- 4  26UH
U 74- 5  0000
(TOTLZ=4625)
U 74- 6  1C5C
U 74- 7  A7CU
U 74- 9  7318
U 74-10  4076
U 74-11  P721
U 74-12  A800
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U 74-13  577U
U 74-14  7F28
U 74-15  PCUF
U 75- 1  26UH
U 75- 2  UF19
(TOTLZ=4625)
U 75- 3  26UH
U 75- 4  UF19
(TOTLZ=4625)
U 75- 5  UF19
(TOTLZ=OFLO)
U 75- 6  UF19
(TOTLZ=4625)
U 75- 8  high
U 75- 9  UF19
(TOTLZ=4625)
U 75-10  high
U 75-11  UF19
(TOTLZ=4625)
U 75-12  0000
U 75-13  UF19
(TOTLZ= OFLO)
U 79- 1  high
U 79- 2  1561
U 79- 3  H636
U 79- 4  U9AF
U 79- 5  PHA9
U 79- 6  2702
U 79- 7  A9F0
U 79- 8  705A
U 79- 9  922C
U 79-11  1F58
U 79-12  H636
U 79-13  U437
U 79-14  H636
U 79-15  315C
U 79-16  FH6H
U 79-17  7450
U 79-18  FH6H
U 79-19  high
U 80- 1  P742
U 80- 2  5684
U 80- 3  FH6H
U 80- 4  AA9H
U 80- 5  H636
U 80- 6  5684
U 80- 7  FH6H
U 80- 8  AA9H
U 80- 9  H636
U 80-11  5684
U 80-12  A9F0
U 80-13  AA9H
U 80-14  H636
U 80-15  5684
U 80-16  FH6H
U 80-17  AA9H
U 80-18  H636
U 80-19  P742
U 81- 1  UF19
(TOTLZ=4625)
U 81- 2  1C5C
U 81- 3  P742
U 81- 4  low
U 81- 5  high
U 81- 6  high
U 81- 8  6P32
U 81- 9  922C
U 81-10  high
U 81-11  3HA6
U 81-12  high
U 81-13  F1CU
U 82- 1  high
U 82- 2  1F58
U 82- 3  FH6H
U 82- 4  high
U 82- 5  H636
U 82- 6  low
U 82- 7  FH6H
U 82- 9  H636
U 82-10  low
U 82-11  PHA9
U 82-12  high
U 82-13  FH6H
U 82-14  high
U 82-15  high
U 83- 1  P742
U 83- 2  C65H
U 83- 3  H636
U 83- 4  AA9H
U 83- 5  FH6H
U 83- 6  C65H
U 83- 7  PHA9
U 83- 8  AA9H
U 83- 9  922C
U 83-11  AA9H
U 83-12  FH6H
U 83-13  C65H
U 83-14  H636
U 83-15  AA9H
U 83-16  FH6H
U 83-17  C65H
U 83-18  H636
U 83-19  P742
```

64602A Timing Acquisition Board
RAM FILLED #8

NORM MODE VH = 38UF

DATA THRESHOLD HIGH: ecl & ttl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: sa gate neg. edge
Location of QUAL/STOP: sa gate pos. edge
Location of CLOCK: sa clk pos. edge
Location of GROUND: gnd

ECL

U 7-12	8505
U 7-13	CHU9
U 7-15	8505
U 11- 3	1AFC
U 11-13	CHU9
U 12- 2	64U3
U 12- 3	5F0U
U 12- 4	5F0U
U 12-14	C91H
U 16-11	78UU
U 16-15	9PP7
U 17- 2	78UU
U 17- 3	HPP4
U 17- 5	9PP7
U 22-26	70UC
U 23-26	70UC
U 24-26	70UC
U 25-26	70UC
U 27- 1	5F0U
U 27- 2	64U3
U 27- 3	70UC
U 27- 4	5F0U
U 27- 5	64U3
U 27- 6	70UC
U 27- 7	1AFC
U 27- 8	9PP7
U 27- 9	high
U 27-10	8505
U 27-11	low
U 27-12	38UF
U 27-13	high
U 27-14	38UF
U 27-15	70UC
U 27-16	64U3
U 27-17	5F0U
U 27-18	70UC
U 27-19	64U3
U 27-20	5F0U
U 27-21	70UC
U 27-22	64U3
U 27-23	5F0U
U 27-24	70UC
U 27-25	64U3
U 27-26	5F0U
U 27-27	38UF
U 27-28	high
U 27-29	38UF
U 27-30	low
U 27-31	HPP4
U 27-32	high
U 27-33	low
U 27-34	high
U 27-35	5F0U
U 27-36	64U3
U 27-37	70UC
U 27-38	5F0U
U 27-39	64U3
U 27-40	70UC
U 29-26	70UC
U 30-26	70UC
U 31-26	70UC
U 32-26	70UC

TTL

U 11- 7		2237
U 11-11		8505
U 12- 5		64U3
U 12- 7		F9P6
U 12-11		C91H
U 16-12		78UU
U 16-13		9PP7
U 22	1	70UC
I	2	70UC
U 23	3	70UC
I	4	70UC
U 31	5	low
I	15	2237
U 32	17	70UC
	18	70UC
	19	70UC
	20	70UC
	21	70UC
	22	70UC
	23	70UC
	24	70UC
	37	70UC
	38	70UC
	39	70UC
	40	70UC
U 24	1	70UC
I	2	70UC
U 25	3	70UC
I	4	70UC
U 29	15	1AFC
I	17	70UC
U 30	18	70UC
	19	70UC
	20	70UC
	21	70UC
	22	70UC

	23	70UC
	24	70UC
	37	70UC
	38	70UC
	39	70UC
	40	70UC
U 33	1	351H
I	2	U519
U 34	3	F50C
I	4	3H26
U 49	5	FF3F
I	6	3F80
U 50	7	4H36
	8	low
	9	70UC
	10	387H
	11	70UC
	12	387H
	13	70UC
	14	387H
	15	70UC
	16	387H
	17	high
	18	CC58
	19	low
	20	38UF
	21	3810
	22	high
U 35	1	351H
I	2	U519
U 36	3	F50C
I	4	3H26
U 51	5	FF3F
I	6	3F80
U 52	7	4H36
	8	low
	9	70UC
	10	387H
	11	70UC
	12	387H
	13	70UC
	14	387H
	15	70UC
	16	387H
	17	high
	18	U602
	19	low
	20	38UF
	21	3810
	22	high
U 37	1	351H
I	2	U519
U 38	3	F50C
I	4	3H26
U 53	5	FF3F
I	6	3F80
U 54	7	4H36
	8	low
	9	70UC
	10	387H
	11	70UC
	12	387H
	13	70UC
	14	387H
	15	70UC
	16	387H
	17	high
	18	0CC2
	19	low
	20	38UF
	21	3810
	22	high
U 39	1	351H
I	2	U519
U 40	3	F50C
I	4	3H26
U 55	5	FF3F
I	6	3F80
U 56	7	4H36
	8	low
	9	70UC
	10	387H
	11	70UC
	12	387H
	13	70UC
	14	387H
	15	70UC
	16	387H
	17	high
	18	014C
	19	low
	20	38UF
	21	3810
	22	high
U 41	1	351H
I	2	U519
U 42	3	F50C
I	4	3H26
U 57	5	FF3F
I	6	3F80
U 58	7	4H36
	8	low
	9	70UC
	10	387H
	11	70UC
	12	387H
	13	70UC
	14	387H
	15	70UC
	16	387H
	17	high
	18	484C
	19	low
	20	38UF
	21	3810
	22	high
U 43	1	351H
I	2	U519
U 44	3	F50C
I	4	3H26
U 59	5	FF3F
I	6	3F80
U 60	7	4H36
	8	low
	9	70UC
	10	387H
	11	70UC
	12	387H
	13	70UC
	14	387H
	15	70UC
	16	387H
	17	high
	18	P1U8
	19	low
	20	38UF
	21	3810
	22	high
U 45	1	351H
I	2	U519
U 46	3	F50C
I	4	3H26
U 61	5	FF3F
I	6	3F80
U 62	7	4H36
	8	low
	9	70UC
	10	387H
	11	70UC
	12	387H
	13	70UC
	14	387H
	15	70UC
	16	387H
	17	high

```
        18   2A7U
        19   low
        20   38UF
        21   3810
        22   high

U 47     1   351H
  |      2   U519
U 48     3   F50C
  |      4   3H26
U 63     5   FF3F
  |      6   3F80
U 64     7   4H36
         8   low
         9   70UC
        10   387H
        11   70UC
        12   387H
        13   70UC
        14   387H
        15   70UC
        16   387H
        17   high
        18   PFA1
        19   low
        20   38UF
        21   3810
        22   high

U 70- 1   low
U 70- 4   C91H
U 70- 5   14A7
U 70- 6   38UF
U 70- 7   2968
U 70- 8   2237
U 70- 9   F22H
U 70-11   F9P6
U 70-12   2237
U 70-13   38UF
U 70-14   0000
U 70-15   64U3
U 70-16   C91H
U 70-19   high
U 72- 1   high
U 72- 2   38UF
U 72- 3   81P1
U 72- 4   C91H
U 72- 5   high
U 72- 6   CHU9
U 72- 7   04P4
U 72- 9   high
U 72-10   high
U 72-11   high
U 72-12   high
U 72-13   04P4
U 72-14   38UF
U 72-15   38UF
(TOTLZ=0125)
U 73- 1   low
U 73- 2   high
U 73- 3   38UF
U 73- 4   3F18
U 73- 5   38UF
U 73- 6   04P4
U 73- 8   CHU9
U 73- 9   38UF
U 73-10   8505
U 73-11   38UF
U 73-12   C91H
U 74- 1   2237
U 74- 2   5A62
U 74- 3   CC64
U 74- 4   91H3
U 74- 5   C91H
U 74- 6   28FP
U 74- 7   CC58
U 74- 9   0CC2
U 74-10   484C
U 74-11   2A7U
U 74-12   PFA1
U 74-13   P1U8
U 74-14   014C
U 74-15   U602
U 75- 1   91H3
U 75- 2   38UF
U 75- 3   91H3
U 76- 1   low
U 76- 2   28CU
U 76- 3   14A7
U 76- 4   14A7
U 76- 5   14A7
U 76- 6   14A7
U 76- 7   CC64
U 76- 8   5A62
U 76- 9   2237
U 76-10   low
U 76-11   04P4
U 76-12   low
U 76-13   38UF
U 76-19   AH15
U 78- 2   C658
U 78- 3   2968
U 78- 4   F22H
U 78- 5   14A7
U 78- 6   14A7
U 78- 7   14A7
U 78- 8   14A7
U 78- 9   14A7
U 78-11   04P4
U 78-12   low
U 78-13   38UF
U 78-19   AH15
U 79- 1   high
U 79- 2   3810
U 79- 3   14A7
U 79- 4   FF3F
U 79- 5   CC64
U 79- 6   3F80
U 79- 7   5A62
U 79- 8   4H36
U 79- 9   2237
U 79-11   3H26
U 79-12   28CU
U 79-13   F50C
U 79-14   14A7
U 79-15   U519
U 79-16   14A7
U 79-17   351H
U 79-18   14A7
U 79-19   high
U 80- 1   1032
U 80- 2   387H
U 80- 3   14A7
U 80- 4   387H
U 80- 5   14A7
U 80- 6   387H
U 80- 7   F22H
U 80- 8   387H
U 80- 9   C658
U 80-11   387H
U 80-12   5A62
U 80-13   387H
U 80-14   14A7
U 80-15   387H
U 80-16   14A7
U 80-17   387H
U 80-18   28CU
U 80-19   1032
U 82- 1   high
U 82- 2   3H26
U 82- 3   14A7
U 82- 4   78UU
U 82- 5   14A7
U 82- 6   9PP7
U 82- 7   14A7
U 82- 9   14A7
U 82-10   low
U 82-11   CC64
U 82-12   high
U 82-13   14A7
U 82-14   high
U 82-15   high
```

U 83- 1	1032
U 83- 2	387H
U 83- 3	14A7
U 83- 4	387H
U 83- 5	14A7
U 83- 6	387H
U 83- 7	CC64
U 83- 8	387H
U 83- 9	2237
U 83-11	387H
U 83-12	14A7
U 83-13	387H
U 83-14	14A7
U 83-15	387H
U 83-16	14A7
U 83-17	387H
U 83-18	2968
U 83-19	1032

64602A Timing Acquisition Board
GALLOPING ONES #9

NORM MODE VH = 4F27

DATA THRESHOLD HIGH: ecl & ttl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: sa gate neg. edge
Location of QUAL/STOP: sa gate pos. edge
Location of CLOCK: sa clk pos. edge
Location of GROUND: gnd

ECL

U 22-26	2317
U 22-35	7PCC
U 23-26	2317
U 23-35	7PCC
U 24-26	2317
U 24-35	7PCC
U 25-26	2317
U 25-35	7PCC
U 27- 1	C01P
U 27- 2	UF39
U 27- 3	2317
U 27- 4	C01P
U 27- 5	UF39
U 27- 6	2317
U 27- 7	249H
U 27- 8	low
U 27- 9	high
U 27-10	low
U 27-11	329F
U 27-12	7PCC
U 27-13	high
U 27-14	7PCC
U 27-15	2317
U 27-16	UF39
U 27-17	C01P
U 27-18	2317
U 27-19	UF39
U 27-20	C01P
U 27-21	2317
U 27-22	UF39
U 27-23	C01P
U 27-24	2317
U 27-25	UF39
U 27-26	C01P
U 27-27	7PCC
U 27-28	high
U 27-29	7PCC
U 27-30	329F
U 27-31	low
U 27-32	high
U 27-33	low
U 27-34	high
U 27-35	C01P
U 27-36	UF39
U 27-37	2317
U 27-38	C01P
U 27-39	UF39
U 27-40	2317
U 29-26	2317
U 29-35	7PCC
U 30-26	2317
U 30-35	7PCC
U 31-26	2317
U 31-35	7PCC
U 32-26	2317
U 32-35	7PCC

TTL

U	4- 1	0000
U	4- 2	6PCC
U	4- 3	0000
U	4- 4	high
U	4- 5	229F
U	4- 6	6PCC
U	4- 7	0059
U	4- 9	4F7P
U	4-10	high
U	4-11	0089
U	4-12	0059
U	4-13	0000
U	4-14	229F
U	4-15	4F27
U 22	1	2317
I	2	2317
U 23	3	2317
I	4	2317
U 31	15	68CA
I	17	2317
U 32	18	2317
	19	2317
	20	2317
	21	2317
	22	2317
	23	2317
	24	2317
	37	2317
	38	2317
	39	2317
	40	2317
U 24	1	2317
I	2	2317
U 25	3	2317
I	4	2317
U 29	15	249H

I	17	2317
U 30	18	2317
	19	2317
	20	2317
	21	2317
	22	2317
	23	2317
	24	2317
	37	2317
	38	2317
	39	2317
	40	2317
U 33	1	75H2
I	2	U9C4
U 34	3	49HC
I	4	0089
U 49	5	AH9F
I	6	3UC6
U 50	7	F7U9
	8	low
	9	2317
	10	753A
	11	2317
	12	753A
	13	2317
	14	753A
	15	2317
	16	753A
	17	high
	18	F82U
	19	low
	20	4F27
	21	8531
	22	high
U 35	1	75H2
I	2	U9C4
U 36	3	49HC
I	4	0089
U 51	5	AH9F
I	6	3UC6
U 52	7	F7U9
	8	low
	9	2317
	10	753A
	11	2317
	12	753A
	13	2317
	14	753A
	15	2317
	16	753A
	17	high
	18	9H37
	19	low
	20	4F27
	21	8531
	22	high
U 37	1	75H2
I	2	U9C4
U 38	3	49HC
I	4	0089
U 53	5	AH9F
I	6	3UC6
U 54	7	F7U9
	8	low
	9	2317
	10	753A
	11	2317
	12	753A
	13	2317
	14	753A
	15	2317
	16	753A
	17	high
	18	PP9H
	19	low
	20	4F27
	21	8531
	22	high
U 39	1	75H2
I	2	U9C4
U 40	3	49HC
I	4	0089
U 55	5	AH9F
I	6	3UC6
U 56	7	F7U9
	8	low
	9	2317
	10	753A
	11	2317
	12	753A
	13	2317
	14	753A
	15	2317
	16	753A
	17	high
	18	C06F
	19	low
	20	4F27
	21	8531
	22	high
U 41	1	75H2
I	2	U9C4
U 42	3	49HC
I	4	0089
U 57	5	AH9F
I	6	3UC6
U 58	7	F7U9
	8	low
	9	2317
	10	753A
	11	2317
	12	753A
	13	2317
	14	753A
	15	2317
	16	753A
	17	high
	18	U5HP
	19	low
	20	4F27
	21	8531
	22	high
U 43	1	75H2
I	2	U9C4
U 44	3	49HC
I	4	0089
U 59	5	AH9F
I	6	3UC6
U 60	7	F7U9
	8	low
	9	2317
	10	753A
	11	2317
	12	753A
	13	2317
	14	753A
	15	2317
	16	753A
	17	high
	18	64AP
	19	low
	20	4F27
	21	8531
	22	high
U 45	1	75H2
I	2	U9C4
U 46	3	49HC
I	4	0089
U 61	5	AH9F
I	6	3UC6
U 62	7	F7U9
	8	low
	9	2317
	10	753A
	11	2317

```
      12  753A
      13  2317
      14  753A
      15  2317
      16  753A
      17  high
      18  4704
      19  low
      20  4F27
      21  8531
      22  high

U 47   1  75H2
  |    2  U9C4
U 48   3  49HC
  |    4  0089
U 63   5  AH9F
  |    6  3UC6
U 64   7  F7U9
       8  low
       9  2317
      10  753A
      11  2317
      12  753A
      13  2317
      14  753A
      15  2317
      16  753A
      17  high
      18  902C
      19  low
      20  4F27
      21  8531
      22  high

U 65- 1   4F27
U 65- 2   0000
U 65- 3   8531
U 65- 4   AH9F
U 65- 5   3UC6
U 65- 6   F7U9
U 65- 7   6538
U 65- 9   6538
U 65-10   14A2
U 65-11   F7U9
U 65-12   3UC6
U 65-13   AH9F
U 65-14   8531
U 65-15   low
U 66- 1   4F27
U 66- 2   0000
U 66- 3   8531
U 66- 4   AH9F
U 66- 5   3UC6
U 66- 6   F7U9
U 66- 7   6538
U 66- 9   6538
U 66-10   14A2
U 66-11   F7U9
U 66-12   3UC6
U 66-13   AH9F
U 66-14   8531
U 66-15   0000
U 67- 1   low
U 67- 2   4FAP
U 67- 3   8531
U 67- 4   05UF
U 67- 5   AH9F
U 67- 6   C593
U 67- 7   3UC6
U 67- 8   39U5
U 67- 9   F7U9
U 67-11   8CHP
U 67-12   75H2
U 67-13   7391
U 67-14   U9C4
U 67-15   P1CC
U 67-16   49HC
U 67-17   F916
U 67-18   0089
U 67-19   low
U 68- 1   4F27
U 68- 2   0000
U 68- 3   0089
U 68- 4   49HC
U 68- 5   U9C4
U 68- 6   75H2
U 68- 7   6538
U 68- 9   6538
U 68-10   high
U 68-11   75H2
U 68-12   U9C4
U 68-13   49HC
U 68-14   0089
U 68-15   14A2
U 69- 1   4F27
U 69- 2   0000
U 69- 3   0089
U 69- 4   49HC
U 69- 5   U9C4
U 69- 6   75H2
U 69- 7   6538
U 69- 9   6538
U 69-10   high
U 69-11   75H2
U 69-12   U9C4
U 69-13   49HC
U 69-14   0089
U 69-15   14A2
U 70- 1   low
U 70- 4   6538
U 70- 5   5694
U 70- 6   4F27
U 70- 7   5694
U 70- 8   68CA
U 70- 9   5694
U 70-11   high
U 70-12   68CA
U 70-13   4F7P
U 70-14   0000
U 70-15   low
U 70-16   6538
U 70-19   high
U 72- 1   high
U 72- 2   4F27
U 72- 3   291U
U 72- 4   6538
U 72- 5   high
U 72- 6   high
U 72- 7   291U
U 72- 9   high
U 72-10   high
U 72-11   high
U 72-12   high
U 72-13   291U
U 72-14   4F27
U 72-15   4F27
(TOTLZ=0125)
U 73- 1   low
U 73- 2   high
U 73- 3   4F27
U 73- 4   6538
U 73- 5   4F27
U 73- 6   291U
U 73- 8   high
U 73- 9   4F27
U 73-10   low
U 73-11   4F27
(TOTLZ=0207)
U 73-12   6538
U 74- 1   68CA
U 74- 2   730U
U 74- 3   373A
U 74- 4   288P
U 74- 5   6538
U 74- 6   4HC6
U 74- 7   F82U
U 74- 9   PP9H
U 74-10   U5HP
U 74-11   4704
U 74-12   902C
U 74-13   64AP
```

```
U 74-14  C06F
U 74-15  9H37
U 75- 1  288P
U 75- 2  4F27
U 75- 3  288P
U 79- 1  high
U 79- 2  8531
U 79- 3  5694
U 79- 4  AH9F
U 79- 5  373A
U 79- 6  3UC6
U 79- 7  730U
U 79- 8  F7U9
U 79- 9  68CA
U 79-11  0089
U 79-12  33AF
U 79-13  49HC
U 79-14  5694
U 79-15  U9C4
U 79-16  5694
U 79-17  964F
U 79-18  5694
U 79-19  high
U 80- 1  0191
U 80- 2  753A
U 80- 3  5694
U 80- 4  753A
U 80- 5  5694
U 80- 6  753A
U 80- 7  5694
U 80- 8  753A
U 80- 9  33AF
U 80-11  753A
U 80-12  730U
U 80-13  753A
U 80-14  5694
U 80-15  753A
U 80-16  5694
U 80-17  753A
U 80-18  33AF
U 80-19  0191
U 81- 2  4HC6
U 81- 3  0191
U 81- 8  249H
U 81- 9  68CA
U 82- 1  high
U 82- 2  0089
U 82- 3  5694
U 82- 4  high
U 82- 5  5694
U 82- 6  low
U 82- 7  5694
U 82- 9  5694
U 82-10  low
U 82-11  373A
U 82-12  high
U 82-13  5694
U 82-14  high
U 82-15  high
U 83- 1  0191
U 83- 2  753A
U 83- 3  5694
U 83- 4  753A
U 83- 5  5694
U 83- 6  753A
U 83- 7  373A
U 83- 8  753A
U 83- 9  68CA
U 83-11  753A
U 83-12  5694
U 83-13  753A
U 83-14  5694
U 83-15  753A
U 83-16  5694
U 83-17  753A
U 83-18  5694
U 83-19  0191
```

NOTES

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section describes adjustments and checks required to return the instrument to peak operating capability after repairs have been made.

5-3. SAFETY REQUIREMENTS.

5-4. Although this instrument has been designed in accordance with international safety standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with precautions listed in the Safety Summary at the front of this manual or with specific warnings given throughout the manual could result in serious injury or death or damage to equipment. Service adjustments should be performed only by qualified service personnel.

5-5. EQUIPMENT REQUIRED.

5-6. a. Digital voltmeter with at least four-place accuracy, such as the HP 3466A DVM, or equivalent.

b. Nonconductive alignment tool.

c. Shorting clip lead.

5-7. DESCRIPTION.

5-8. The 64602A timing acquisition board has only three adjustments, one for DAC negative full-scale, and two for DAC positive full-scale.

5-9. PV tests 1 and 2 are used to make the DAC adjustments.

5-10. KEYBOARD SETUP.

5-11. Use the following steps to access the 64602A Acquisition Board PV tests, which are used to make the DAC adjustments:

a. With the operating system initialized and awaiting a command, press the softkey labeled "opt_test" (you may have to keep pressing the "etc" softkey until you see "opt_test" on the screen).
b. Press [RETURN]. You should see a listing of all the optional boards that are present in your mainframe, along with their slot numbers.
c. Type in the Timing Acquisition Board slot number.
d. Press [RETURN].
e. Press softkey "run".
f. Press softkey "slot".
g. Type in the Timing Acquisition Board slot number.
h. Press softkey "test". The screen will now list all the Timing Acquisition Board PV tests.
i. Type in the number of the test you wish to run. (For the acquisition board adjustments, use tests 1 and 2).
j. Press [RETURN].

5-12. DACS NEGATIVE FULL-SCALE ADJUSTMENT.

5-13.

a. Disconnect the timing probe from the acquisition board before making this adjustment.

b. If it has not already been done, press softkey "opt_test", [RETURN], and then the following softkeys in sequence: "run slot (type in acq. bd. slot) test 1".

c. Press [RETURN]

d. Connect the ground lead of the DVM to the GND test point located on the upper middle part of the board.

e. Short TP1 to TP2 with the clip lead.

f. Connect the V-ohms lead of the DVM to TP1.

g. Adjust -FS (R2) for -2.133V +/- 0.5mV at TP1.

h. Remove the clip lead shorting TP1 to TP2.

i. Check that TP1 and TP2 are within 4.0mv of each other; if they are they are not, suspect U77 (op-amp) within the DAC circuitry.

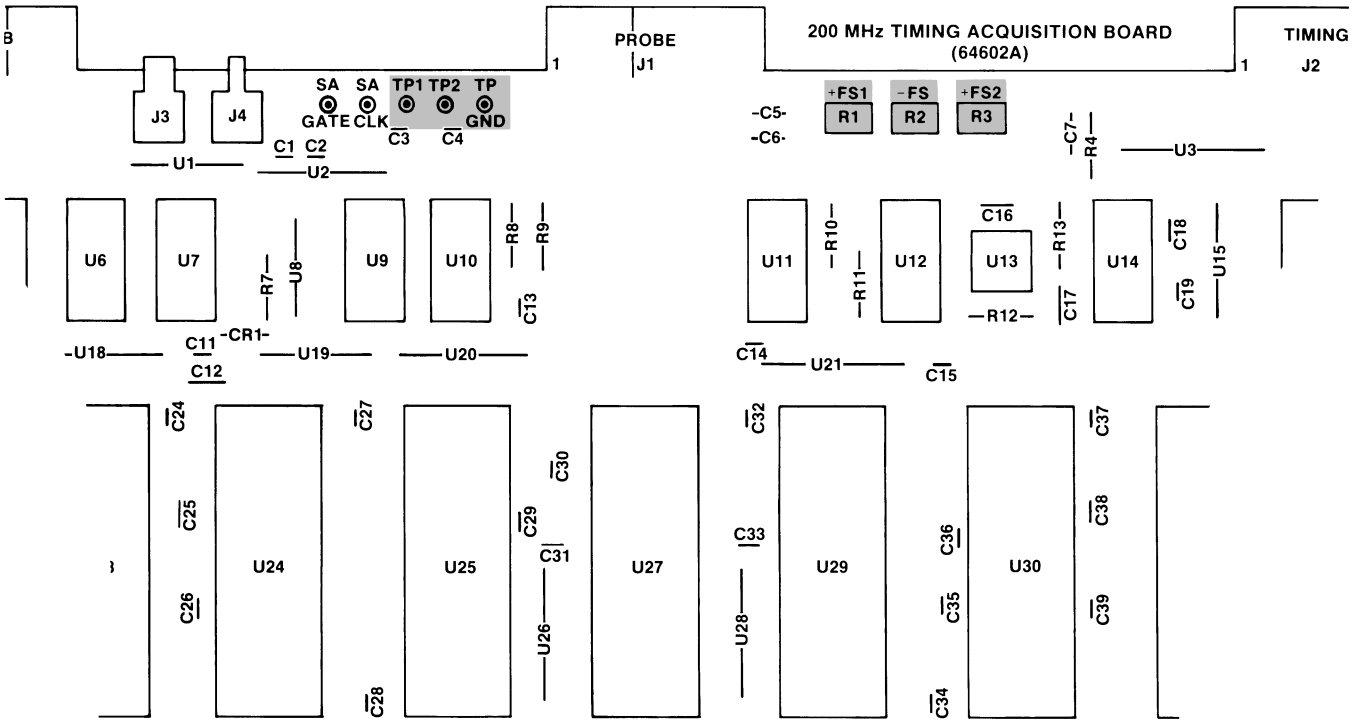


Figure 5-1. Adjustments

5-14. DACS POSITIVE FULL-SCALE ADJUSTMENT.

5-15. a. Disconnect the timing probe from the acquisition board before making this adjustment.

b. If it has not already been done, press softkey "opt_test", [RETURN], and then the following softkeys in sequence: "run slot (type in acq. bd. slot) test 2".

c. Press [RETURN].

d. Connect the ground lead of the DVM to the GND testpoint located on located on the upper middle part of the board.

e. Connect the V-ohms lead of the DVM to TP1.

f. Adjust +FS1 (R1) for +2.117V +/- 0.5mV at TP1.

g. Connect the V-ohms lead of the DVM to TP2.

h. Adjust +FS2 (R3) for +2.117V +/- 0.5mV at TP2.

NOTES

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five-digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used: one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lower-case and upper-case letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Chassis-mounted parts are in alphanumerical order by reference designation.

b. Electrical assemblies and their components in alphanumerical order by reference designation.

c. Miscellaneous parts.

The information given for each part consists of the following:

a. The Hewlett-Packard part number and the check digit.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A five-digit code that indicates the manufacturer.

e. The manufacturer's part number.

The total quantity for each part is given only once, at the first appearance of the part number in the list.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-9. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-10. SPARE PARTS KIT.

6-11. A service kit is available. To order, please contact your local sales and service representative.

6-12. DIRECT MAIL ORDER SYSTEM.

6-13. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount, for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

6-14. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	assembly	**F**	fuse	**MP**	mechanical part	**U**	integrated circuit
B	motor	**FL**	filter	**P**	plug	**V**	vacuum, tube, neon bulb, photocell, etc
BT	battery	**IC**	integrated circuit	**Q**	transistor		
C	capacitor	**J**	jack	**R**	resistor	**VR**	voltage regulator
CP	coupler	**K**	relay	**RT**	thermistor	**W**	cable
CR	diode	**L**	inductor	**S**	switch	**X**	socket
DL	delay line	**LS**	loud speaker	**T**	transformer	**Y**	crystal
DS	device signaling (lamp)	**M**	meter	**TB**	terminal board	**Z**	tuned cavity network
E	misc electronic part	**MK**	microphone	**TP**	test point		

ABBREVIATIONS

A	amperes	**H**	henries	**N/O**	normally open	**RMO**	rack mount only
AFC	automatic frequency control	**HDW**	hardware	**NOM**	nominal	**RMS**	root-mean square
AMPL	amplifier	**HEX**	hexagonal	**NPO**	negative positive zero (zero temperature coefficient)	**RWV**	reverse working voltage
		HG	mercury				
BFO	beat frequency oscillator	**HR**	hour(s)				
BE CU	beryllium copper	**HZ**	hertz	**NPN**	negative positive-negative	**S-B**	slow-blow
BH	binder head					**SCR**	screw
BP	bandpass			**NRFR**	not recommended for field replacement	**SE**	selenium
BRS	brass	**IF**	intermediate freq			**SECT**	section(s)
BWO	backward wave oscillator	**IMPG**	impregnated	**NSR**	not separately replaceable	**SEMICON**	semiconductor
		INCD	incandescent			**SI**	silicon
CCW	counter-clockwise	**INCL**	include(s)			**SIL**	silver
CER	ceramic	**INS**	insulation(ed)	**OBD**	order by description	**SL**	slide
CMO	cabinet mount only	**INT**	internal	**OH**	oval head	**SPG**	spring
COEF	coeficient			**OX**	oxide	**SPL**	special
COM	common	**K**	kilo 1000			**SST**	stainless steel
COMP	composition					**SR**	split ring
COMPL	complete	**LH**	left hand	**P**	peak	**STL**	steel
CONN	connector	**LIN**	linear taper	**PC**	printed circuit		
CP	cadmium plate	**LK WASH**	lock washer	**PF**	picofarads 10^{-12} farads	**TA**	tantalum
CRT	cathode-ray tube	**LOG**	logarithmic taper			**TD**	time delay
CW	clockwise	**LPF**	low pass filter	**PH BRZ**	phosphor bronze	**TGL**	toggle
				PHL	phillips	**THD**	thread
DEPC	deposited carbon	**M**	milli 10^{-3}	**PIV**	peak inverse voltage	**TI**	titanium
DR	drive	**MEG**	meg 10^{6}	**PNP**	positive-negative-positive	**TOL**	tolerance
		MET FLM	metal film			**TRIM**	trimmer
ELECT	electrolytic	**MET OX**	metallic oxide	**P/O**	part of	**TWT**	traveling wave tube
ENCAP	encapsulated	**MFR**	manufacturer	**POLY**	polystyrene		
EXT	external	**MHZ**	mega hertz	**PORC**	porcelain	**U**	micro 10^{-6}
		MINAT	miniature	**POS**	position(s)		
F	farads	**MOM**	momentary	**POT**	potentiometer	**VAR**	variable
FH	flat head	**MOS**	metal oxide substrate	**PP**	peak-to-peak	**VDCW**	dc working volts
FIL H	fillister head	**MTG**	mounting	**PT**	point		
FXD	fixed	**MY**	"mylar"	**PWV**	peak working voltage	**W/**	with
						W	watts
G	giga (10^{9})	**N**	nano (10^{-9})	**RECT**	rectifier	**WIV**	working inverse voltage
GE	germanium	**N/C**	normally closed	**RF**	radio frequency		
GL	glass	**NE**	neon	**RH**	round head or right hand	**WW**	wirewound
GRD	ground(ed)	**NI PL**	nickel plate			**W/O**	without

Table 6-2. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64602A	0		TIMING ANALYSIS ACQUISITION BOARD	28480	64602A
A1	64602-66503	2		200 MHZ TIMING ANALYSIS BOARD	28480	64602-66503
A1C1	0160-4385	2	1	CAPACITOR-FXD 15PF +-5% 200VDC CER 0+-30	28480	0160-4385
A1C2	0160-4383	0	1	CAPACITOR-FXD 6.8PF +-.5PF 200VDC CER	20932	5024E0200RD689D
A1C3	0160-3879	7	47	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C5	0160-3443	1	5	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C6	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C7	0140-0151	0	3	CAPACITOR-FXD 820PF +-2% 300VDC MICA	72136	DM15F821G0300WV1CR
A1C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C9	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C11	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C12	0140-0151	0		CAPACITOR-FXD 820PF +-2% 300VDC MICA	72136	DM15F821G0300WV1CR
A1C13	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C14	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C15	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C16	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C17	0140-0151	0		CAPACITOR-FXD 820PF +-2% 300VDC MICA	72136	DM15F821G0300WV1CR
A1C18	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C20	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C21	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C22	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C23	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C24	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C25	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C26	0180-2255	3	2	CAPACITOR-FXD 2.2UF+-20% 20VDC TA	28480	0180-2255
A1C27	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C28	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C29	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C30	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C31	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C32	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C33	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C34	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C35	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C36	0180-2255	3		CAPACITOR-FXD 2.2UF+-20% 20VDC TA	28480	0180-2255
A1C37	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C38	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C39	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C40	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C41	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C42	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C43	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C44	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C45	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C46	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C47	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C48	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C49	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C50	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C51	0160-5338	7	1	CAPACITOR-FXD .33UF +-10% 50VDC CER	28480	0160-5338
A1C52	0160-2306	3	2	CAPACITOR-FXD 27PF +-5% 300VDC MICA	28480	0160-2306
A1C53	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C54	0160-2306	3		CAPACITOR-FXD 27PF +-5% 300VDC MICA	28480	0160-2306
A1C55	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C56	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C57	0180-1746	5	5	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C58	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C59	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C60	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C61	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C62	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C63	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C65	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C66	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C67	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C68	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C69	0160-4492	5	2	CAPACITOR-FXD 18PF +-5% 200VDC CER	51642	200-200-NPO-180J
A1C70	0160-4492	5		CAPACITOR-FXD 18PF +-5% 200VDC CER	51642	200-200-NPO-180J

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1CR1	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR3	1901-0535	9	2	DIODE-SM SIG SCHOTTKY	28480	1901-0535
A1CR4	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A1J3	1250-1189	0	1	CONNECTOR-RF SMB FEM PC 50-OHM	28480	1250-1189
A1J4	1250-0543	8	1	CONNECTOR-RF SM-SNP M PC 50-OHM	28480	1250-0543
A1MP1	0520-0133	4	2	SCREW-MACH 2-56 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1MP2	1205-0461	4	1	HEAT SINK	28480	1205-0461
A1MP3	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
A1MP4	2190-0014	1	2	WASHER-LK INTL T NO. 2 .089-IN-ID	28480	2190-0014
A1MP5	4320-0095	7		U CHANNEL NPRN .047-WD-CHAN .219-WD.	28480	4320-0095
A1MP6	64602-21102	5	1	HEAT SINK-COVER	28480	64602-21102
A1MP7	64602-25001	7	1	BOARD EJECTOR	28480	64602-25001

Table 6-2. Replaceable Parts List (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U21	1810-0271	7		NETWORK-RES 10-SIP200.0 OHM X 9	01121	210A201
A1U22	1NB4-5017	7	8	IC-ENCODER	28480	1NB4-5017
A1U23	1NB4-5017	7		IC-ENCODER	28480	1NB4-5017
A1U24	1NB4-5017	7		IC-ENCODER	28480	1NB4-5017
A1U25	1NB4-5017	7		IC-ENCODER	28480	1NB4-5017
A1U26	1810-0538	9		NETWORK-RES 9-SIP MULTI-VALUE	28480	1810-0538
A1U27	1NB4-5007	8	1	IC-GLITCH DETECTOR	28480	1NB4-5007
A1U28	1810-0538	9		NETWORK-RES 9-SIP MULTI-VALUE	28480	1810-0538
A1U29	1NB4-5017	7		IC-ENCODER	28480	1NB4-5017
A1U30	1NB4-5017	7		IC-ENCODER	28480	1NB4-5017
A1U31	1NB4-5017	7		IC-ENCODER	28480	1NB4-5017
A1U32	1NB4-5017	7		IC-ENCODER	28480	1NB4-5017
A1U64	1816-1476	8	32	IC TTL 1024 (1K) STAT RAM 45-NS 3-S	28480	1816-1476
A1U65	1820-2890	6	4	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U66	1820-2890	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U67	1820-1917	1	4	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A1U68	1820-2890	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U69	1820-2890	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U70	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A1U71	1820-1282	3	1	IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
A1U72	1820-1245	8	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS155N
A1U73	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U74	1820-2550	0	1	IC DCDR TTL LS 3-TO-8-LINE	01295	SN74LS137N
A1U75	1820-2657	8	1	IC GATE TTL ALS OR QUAD 2-INP	01295	SN74ALS32N
A1U76	1826-0856	7	2	IC CONV 8-B-D/A 20-DIP-P PKG	34335	AM6080APC
A1U77	1826-0974	5	1	IC OP AMP GP DUAL 14-DIP-C PKG	07263	UA747DM
A1U78	1826-0856	7		IC CONV 8-B-D/A 20-DIP-P PKG	34335	AM6080APC
A1U79	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A1U80	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A1U81	1820-2656	7	1	IC GATE TTL ALS NAND QUAD 2-INP	01295	SN74ALS00N
A1U82	1820-1492	7	1	IC BFR TTL LS INV HEX 1-INP	01295	SN74LS368AN
A1U83	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A1XU22	1200-0654	7	8	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU23	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU24	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU25	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU27A	1200-0963	1	2	PIN-SOCKET-20	28480	1200-0963
A1XU27B	1200-0963	1		PIN-SOCKET-20	28480	1200-0963
A1XU29	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU30	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU31	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU32	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU64	1200-0612	7	32	SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU67	1200-0639	8	7	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU70	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU72	1200-0607	0	3	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU74	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU75	1200-0638	7	2	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1XU76	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU78	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU79	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU80	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU81	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1XU82	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU83	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
W1	64600-61601	1	2	CABLE-RF	28480	64600-61601
W2	64604-61601	5	1	CABLE-PROBE	28480	64604-61601

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
S0167	FUJITSU LTD	TOKYO	JP	
S4013	HITACHI	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND	CA	91745
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
11236	CTS OF BERNE INC	BERNE	IN	46711
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
20932	EMCON DIV ITW	SAN DIEGO	CA	92129
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
25403	AMPEREX ELEK CORP SEMICON & MC DIV	SLATERSVILLE	RI	02876
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
27167	CORNING GLASS WORKS (WILMINGTON)	WILMINGTON	NC	28401
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
52763	STETTNER-TRUSH INC	CAZENOVIA	NY	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP	FLORENCE	SC	06226
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA	PA	19108

See introduction to this section for ordering information

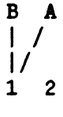
NOTES

SECTION VII

MANUAL CHANGES

7-1. This section normally contains information for backdating this manual for models with repair numbers prior to the one shown on the title page. This edition includes information for the first repair number, so there would ordinarily be no backdating material. However some of the earliest customers received a Revision A board, which is somewhat different from the presently shipped Revision B board.

7-2. The Rev A board only, has a small pair of soldered jumpers at the very bottom left-hand corner (when viewing from the component side). Both A and B on these jumpers must be connected to 1, as shown.



7-3. Two 2.2 uF capacitors were changed to .01 uF capacitors. On the REV A component locator, shown below, these were C26 and C36. In comparing this old locator with the present one, you will notice the positions of the capacitors next to the encoders have changed. C26 has become C24 and is connected between +5V and ground. C36 is unconnected. A listing of the .01 uF capacitors next to the encoders (U22-27, U29-32) on the REV A board is given:

C22,23,25,26,28,29,34-36,38-40 are connected from +5V to ground.

C24,27,30,32,37,41 are connected from -3.25V to ground.

C31,33 are connected from -5.2V to ground.

7-4. The capacitor connections on the REV B board are given on Service Sheet 1 of Section 8. Capacitor positions for the REV B board are shown on the component locators in this manual.

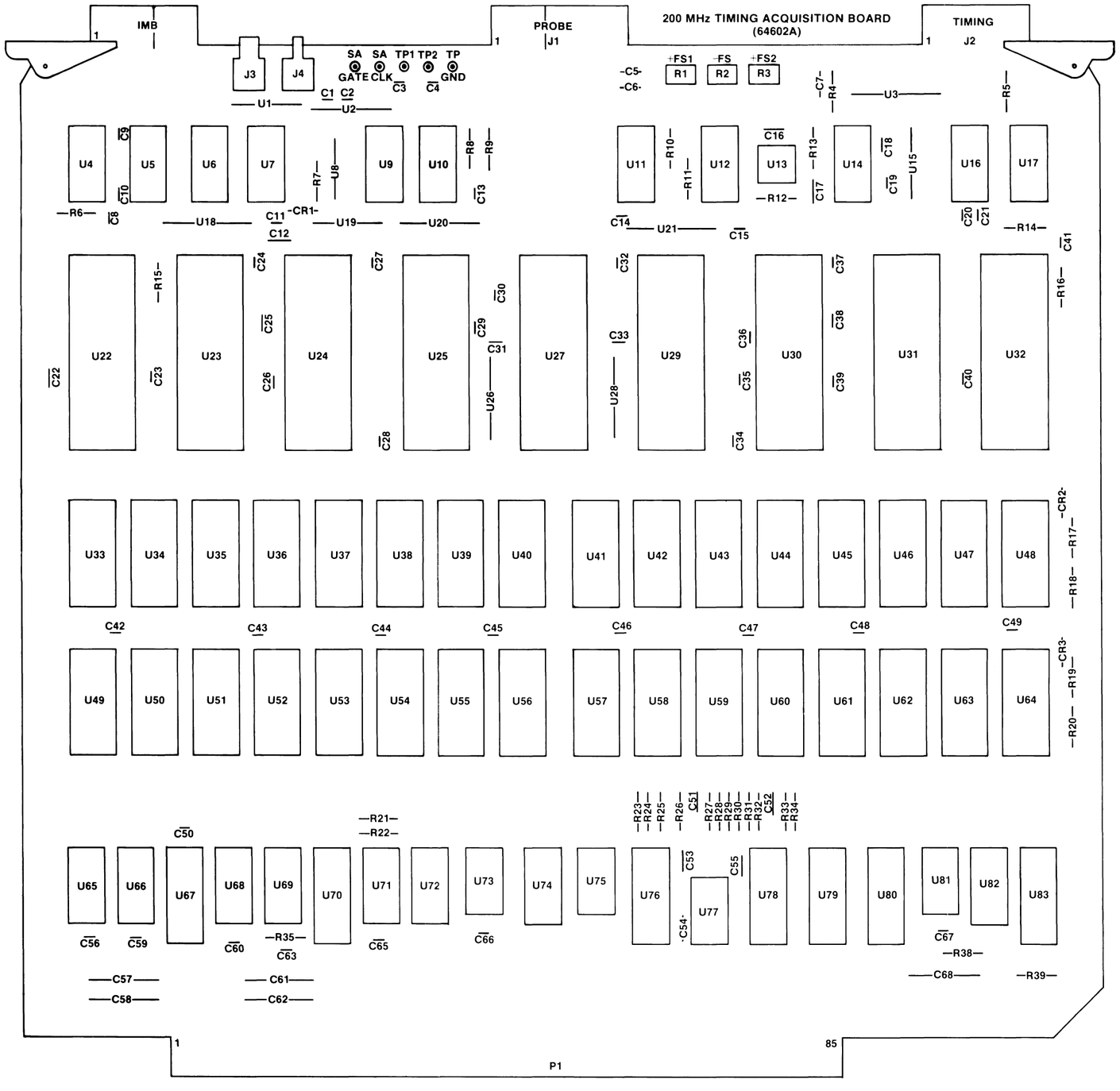


Figure 7-1. REV A Component Locator.

SECTION VIII

THEORY AND SCHEMATICS

CAUTION

THE GLITCH (U27) AND ENCODER (U22-25, U29-32) CHIPS ARE VERY SENSITIVE TO STATIC. THEY SHOULD BE LEFT IN CONDUCTIVE FOAM UNTIL INSTALLATION. GROUNDING STRAPS AND A GROUNDED WORK STATION ARE RECOMMENDED WHEN HANDLING THE ICS.

8-1. INTRODUCTION.

8-2. This section contains block diagrams, mnemonic tables, schematics and theory. Some theory is also given with the PV test descriptions in SECTION 4.

8-3. There are four modes of timing analyzer operation: Wide Channel, in which eight channels are sampled at a 200MHz rate and stored as 4096 bits of serial data per channel; 4-Channel Glitch Capture Mode which identifies multiple transitions between clock pulses, with both 4K of data and 4K of glitch information stored per channel; 4-Channel Dual Threshold Mode in which four channels are compared to two thresholds, and 4K is stored for each threshold on each channel; 4-Channel Fast Sample Mode in which four channels are sampled in a time-interleaved fashion for an effective 400MHz sample rate, and 8K of data is stored for each channel.

8-4. PROBE THEORY.

8-5. The probe bus passes data from the system under test to the analyzer via the 64604A timing probe. The probe compares the voltages on inputs 0-3 and 4-7 to a corresponding pair of d.c. thresholds from two D/A converters on the acquisition board. The DACs supply middle thresholds to the probe in the wide sample, glitch, and fast sample modes. In the dual threshold mode the DACs supply both upper and lower thresholds.

8-6. GLITCH CHIP. (Figs. 8-1, 8-8)

8-7. The glitch chip (U27) receives timing data from the probe. The glitch chip contains a 20-bit holding register which is programmed by the mainframe for a specified trigger pattern and mode of operation, as follows:

Bit 1: Chooses recognition of either pattern, or pattern complement.
Bit 2: Chooses synchronous triggering, in which the pattern is compared with already sampled data, rather than with the asynchronous incoming data. This is used for glitch triggering, which is by definition synchronous, ie, referenced to sample times.
Bit 3: Chooses either data sampling from all probes, or, in the glitch mode, from only the four low-order probes (0-3), which are then used for both data and glitch information.
Bit 4: Don't care.
Bits 5-20: Each pair of bits defines the trigger condition on a different channel, as follows:

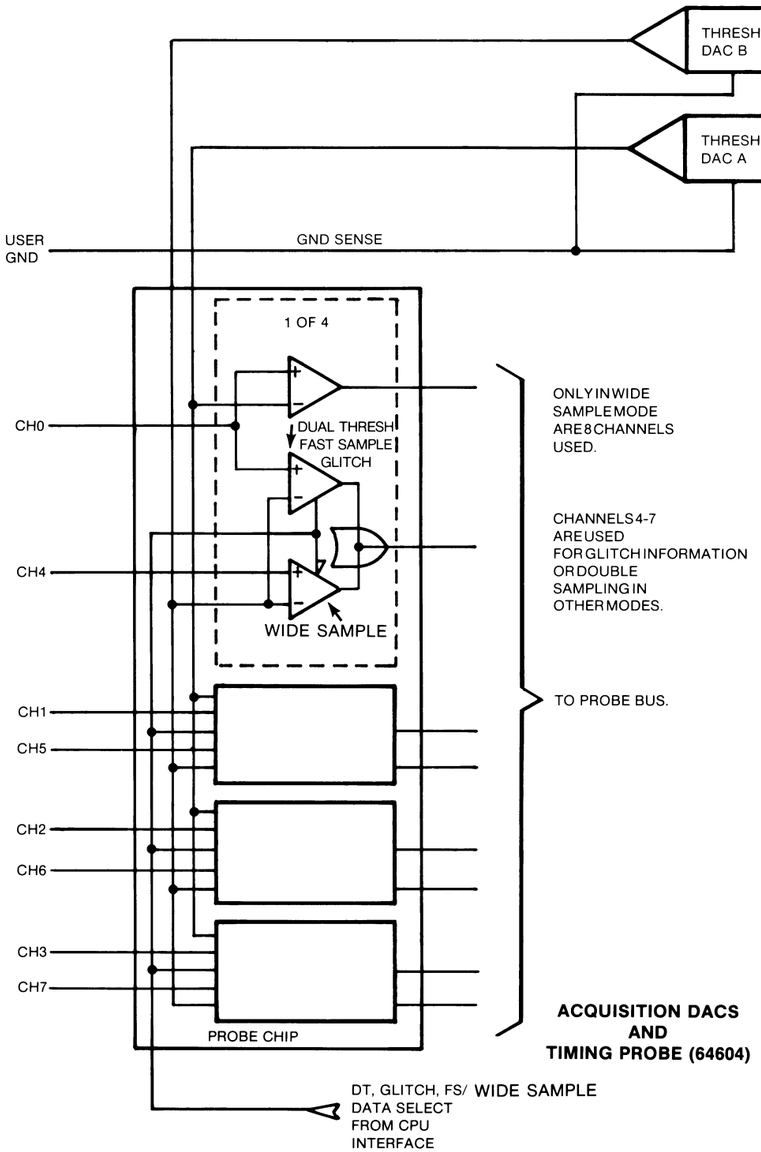
A	B	
0	0	Always trigger, ie, don't care.
0	1	Trigger on a high signal.
1	0	Trigger on a low signal.
1	1	Never trigger, ie, not don't care.

8-8. The glitch chip samples incoming probe data on both edges of the sample clock from the analyzer Control Board. Since both clock edges are used, at the 200MHz maximum sample rate the clock need only be 100MHz. Two pairs of complementary clock signals go into the glitch chip: HE/phi2A, LE/phi2A, HE/phi2B, and LE/phi2B. The "A" clocks differ from each other by 180 degrees, as do the "B" clocks. "A" and "B" clocks are identical except in the Fast Sample Mode, when the "B" clock is delayed by 2.5ns to double the number of sample edges.

8-9. In Fast Sample Mode the control bit to the probe is set, as in dual threshold mode, to doubly compare channels 0-3; but now both threshold voltages are set to the same value. This produces two outputs per channel; and with four separate clock sampling times instead of two, the sample rate is effectively 400MHz.

8-10. In Dual Threshold Mode a control bit to the probe connects the Ch. 0-3 inputs to two comparators. Each of the four inputs is compared to two thresholds from the acquisition board D/A converters. The lower threshold comparisons come into the glitch chip on channels 0-3, and the upper ones on channels 4-7. Software unscrambles the four pairs of data streams into a 3-level signal on four channels--high, middle, and low.

8-11. In Glitch Mode the glitch chip ignores data on channels 4-7 but performs normal sampling plus glitch capture on channels 0-3. Glitches are detected by looking for transitions which conflict with sampled data, such as positive-then-negative transitions after the data was found to be low during the previous sample time.



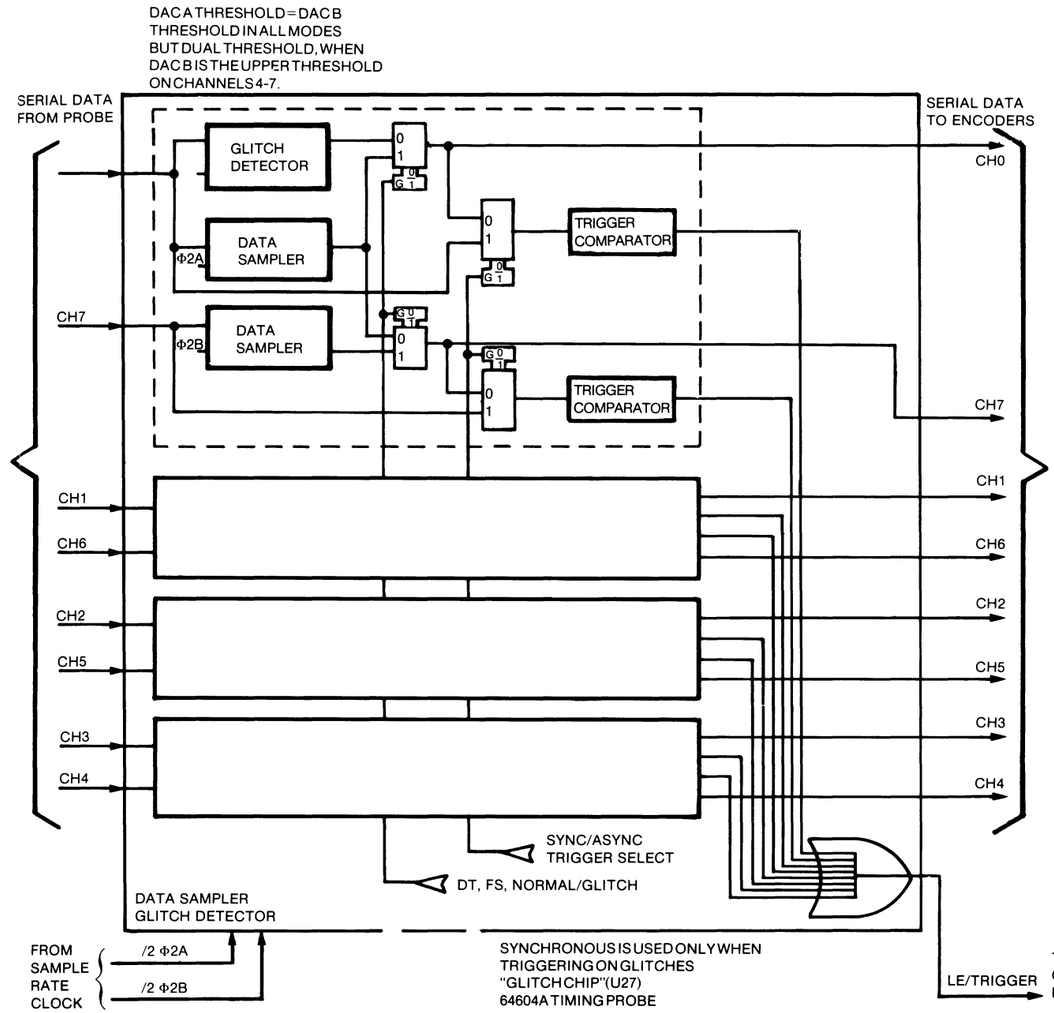


Figure 8-1.
64604A Probe & the "Glitch Chip" Block Diagram
ACQ 8-3

GLITCH CHIP (continued)

8-12. Since a glitch is by definition a synchronous event--an event bounded by sampling times--triggering on a glitch must be synchronous also. Triggering then occurs only with reference to sample times. When glitches are to be captured only, and not used for triggering, the pattern recognition circuitry is left in its asynchronous mode. Triggering then occurs whenever incoming data conforms to the specified pattern, regardless of whether or not this happens at sample time. The glitch and data information for each of the four channels is processed by the glitch chip as two separate channels would be in the wide channel mode, and the software recombines them into one channel with both glitch and data attributes.

8-13. When the glitch chip finds a match between its pattern and the data on all channels, it will emit an active Low trigger signal, LE/TRIG, for the duration of the match, or until it is reset. XE/TRIG, derived from LE/TRIG, may be programmed High or Low true by the trigger polarity signal, XE/TRIGPOL. A High trigger is used in ANDing a High trigger from another acquisition board; Low triggers are used for ORing. Trigger polarity can also determine whether transition triggering will occur on an "entering" or "leaving" pattern.

8-14. SERIAL-TO-PARALLEL ENCODERS. (Figs. 8-2, 8-8)

8-15. The encoders change the serial stream for each channel from the glitch chip to a pair of 8-bit parallel loads for the RAM.

[redacted]

loaded at the sample clock rate. When a register is full it feeds eight parallel bits to the RAM; then the other register is loaded and unloaded.

8-17. Write pulses for the RAM and clocking pulses for the memory address counters are derived in only one encoder (U22) by dividing the sample clock rate by eight. Thus, acquisition memory need not be especially fast, but can operate at one-sixteenth of 200MHz. The write pulses are out of phase from each other by one-half clock period.

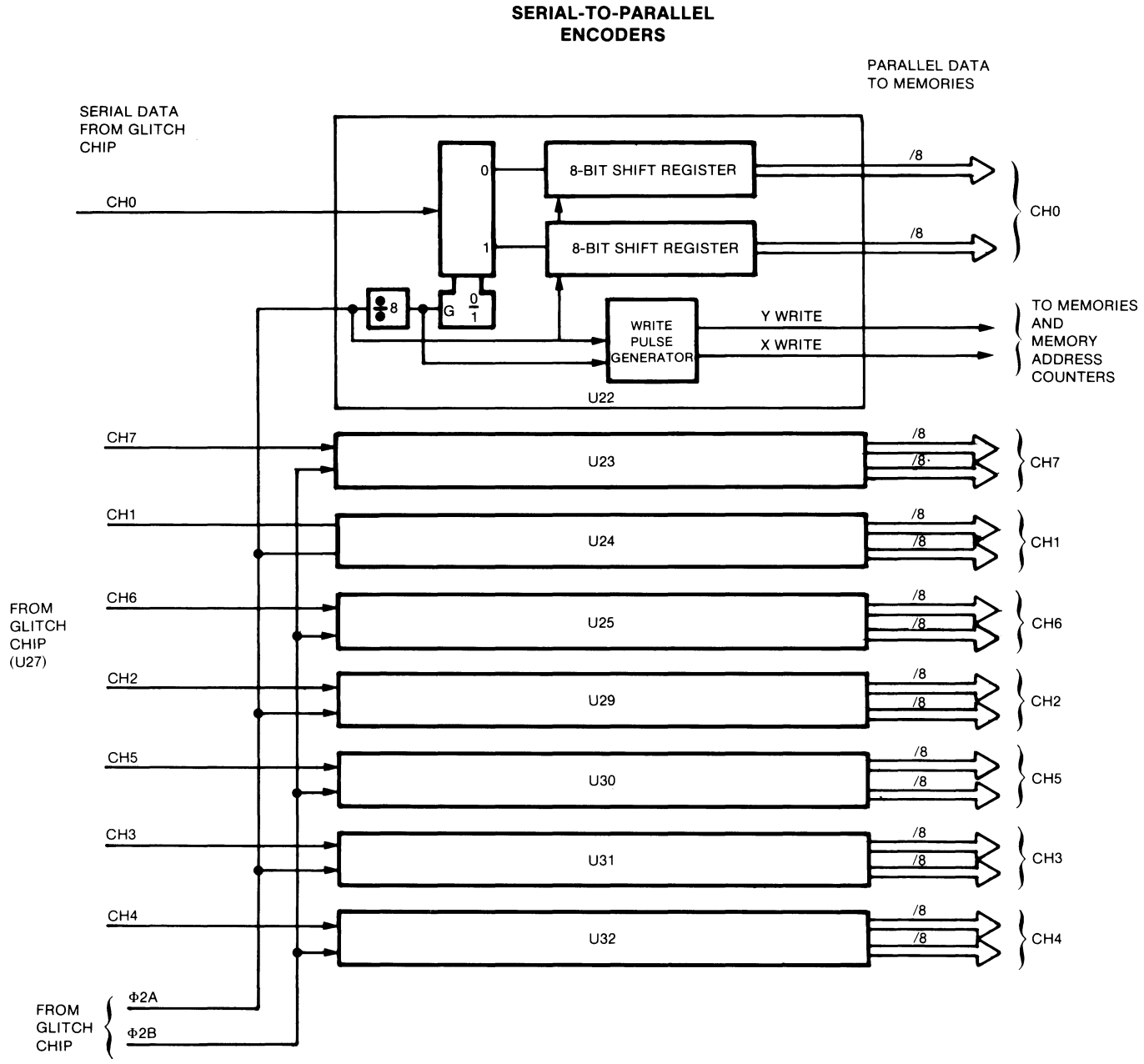


Figure 8-2.
Serial-to-Parallel Encoders
Block Diagram

8-21. MEMORY ADDRESS COUNTERS (MACs). (Fig. 8-6)

8-22. There are two counters, one for "X" memory bank addresses, and one for the "Y" memory bank. After being set to zero before a run by HE/RESET, the MACs are clocked by write pulses (derived from the sample clock and divided by eight) from one of the encoders. Since they are driven by asymmetrical clocks with a fixed phase relationship, the counters differ at most by one count, with the X counter leading.

8-23. A wrap-around latch (U4) which receives the terminal count and the least significant bit of the Y counter, indicates by H/MEMFUL when the memory has been completely filled with new data at least once.

8-24. The window counter on the analyzer Control Board ends the trace a programmed number of sample clocks after tracepoint. Since the trace is ended by stopping the sample clock, the MACs are also stopped. By reading this end-of-trace address, and the three trigger position bits (H/TC0-2) the mainframe CPU can find where tracepoint occurs in memory.

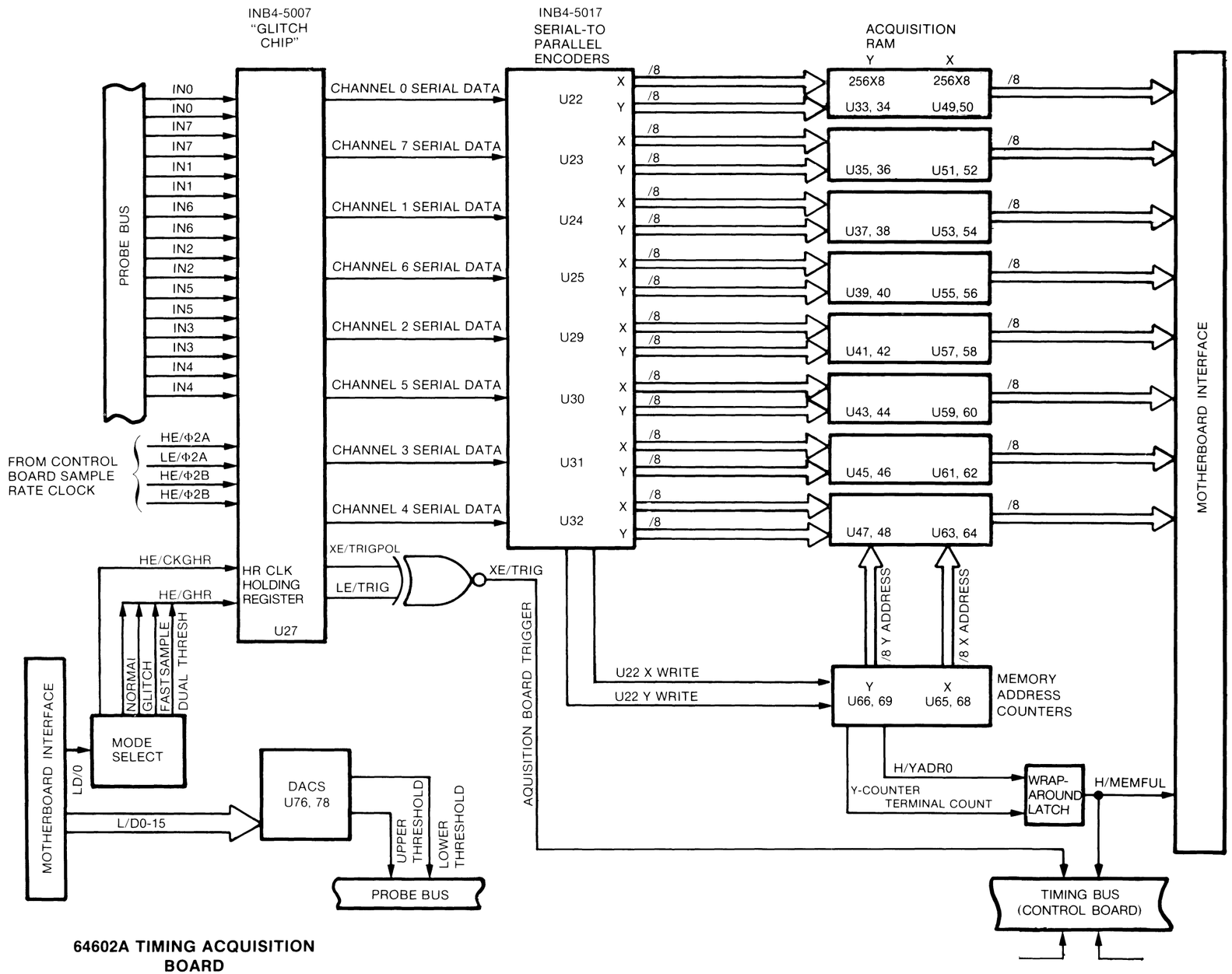
8-25. The "window" programmed into the control board window counter determines trigger position in memory. The "window" is amount of memory between tracepoint and the end-of-acquisition. For example, in our 4K system, if tracepoint occurs at address 3000 (decimal) and the window counter stops acquisition 10 addresses later, then displayed pre-trigger information will begin at address 3011, continue through 4095, and end at 2999. The window, from tracepoint to the end of trace, will be 10 locations; and displayed pre-trigger memory will consist of 4085 locations. (Actually, only 4060, or 8140, bits are displayed).

8-26. The following steps occur in a acquisition run:

a. Before an acquisition run, the MACs and encoders are reset.
b. A run begins and memory fills, with the MACs counting addresses.
c. Tracepoint may or may not occur before the memory is filled once.
d. When tracepoint occurs, the Control Board window counter will count down from a programmed delay, finally stopping acquisition and the MACs.
e. When acquisition is stopped, the CPU will read the last address to which data was written by reading the X address, the least significant Y address bit, and the trigger enable counter on the Control Board.

8-27. DIGITAL/ANALOG CONVERTERS (DACs). (Fig. 8-7)

8-28. The DACs set the middle threshold for the probes in the Wide Sample, Glitch, and Fast Sample Modes. In Dual Threshold Mode, DAC A (U76) sets the lower threshold, using channels 0-3; and DAC B (U78) sets the upper threshold, using channels 4-7.



64602A TIMING ACQUISITION BOARD

Figure 8-3.
64602A Timing Acquisition Board
Block Diagram

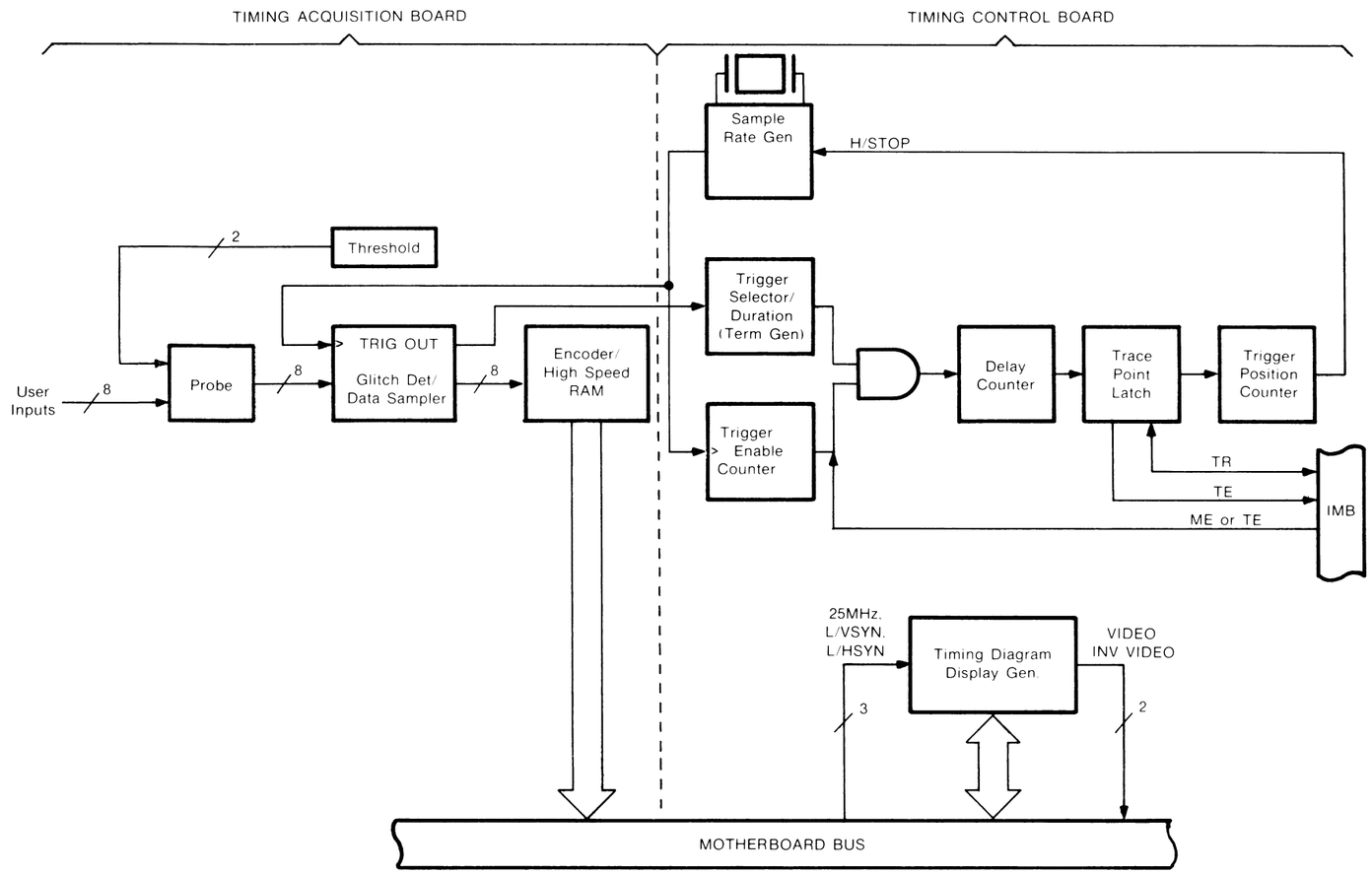


Figure 8-4.
Timing Analysis System
Block Diagram
ACQ 8-8

8-29. LOGIC CONVENTION

8-30. Logic states are defined as follows:

0----------False, negated, inactive, or unasserted state.

1----------True, active, or asserted state.

8-31. Voltage levels representing logic states:

LOW (L)--------The more negative of two voltage levels.

HIGH (H)-------The more positive of two voltage levels.

8-32. Signals may be either high true, or low true, as indicated by the mnemonics on the service sheets.

8-33. The 64602A includes both TTL and ECL ICs. Worst case voltage levels for trouble shooting and signature analysis purposes are as follows: (IC data sheet specifications may be better than this).

TTL Voltage Levels

Level	Voltage
LOW	<0.8
HIGH	>2.0

ECL Voltage Levels

Level	Voltage
LOW	<-1.50
HIGH	>-1.10

8-34. MNEMONICS.

8-35. Mnemomic definitions are listed in Table 8-1 in the alphabetical order of characters after the slash. The following convention is used:

a. An L or H before the slash indicates active LOW or HIGH.
b. An E after L or H, but before the slash, indicates an ECL signal.
c. No E before the slash indicates a TTL signal.
d. An X instead of L or H means the signal may be programmed as either active LOW or HIGH.
e. The functional mnemonic appears after the slash.

Table 8-1. Mnemonics

MNEMONIC	DEFINITION	SCHEMATICS	ORIGIN
L/A0-15	Address lines from mother-board.	1,2	1
H/BD0	Buffered data-line 0 from mother-board.	1,4	1
HE/CKGHR	Clock to glitch chip holding register.	1,4	1
L/D0-15	Data lines from mother-board.	1,3,5	1
HE/DT	Enable dual-threshold mode.	1,3	1
L/ENDAC	Enable D/A converters.	1,4	1
HE/ENFAST	Enable fast-sample mode.	1,4	1
H/ENTEST	Enable test.	1,4	1

MNEMONIC	DEFINITION	SCHEMATICS	ORIGIN
HE/GHR	Glitch holding register data.	1,4	1
L/IDBD	Identify board, derived from L/ID.	1,3	1
HE/PROBE 0-7 LE/PROBE 0-7	Inputs and inverse inputs from probe.	3,4	3
H/INIT	Initializes encoders. Derived from HE/RESET.	3,4	3
L/LOADCTR	Load counter. Enable loading memory adddress counters.	1,2	1
H/MEMFUL	Memory full. Indicates that memory has been loaded with good data at least once.	2,3	2
L/OERAM0-7	Output enable RAM.	1,5	5
L/STBBD	Strobe board, derived from L/SELBD.	1,3	1
H/RAMOUT0-15	RAM output.	5	5
L/RESETCTR	Reset address counters.	2,3	3
HE/RUN	Enables run mode.	2,3	3
L/WRTY	Enables write to Y memory bank.	2,5	2
HE/phi2 LE/phi2	Sample rate clocks from the control board.	2	2
LE/phi2A * HE/phi2A * HE/phi2B * LE/phi2B *	Buffered sample clocks to the glitch chip.	2,4	1
L/READCTR	Read counter. Enables reading memory address counter.	1,5	1
L/READRAM	Read RAM. Enables reading acquisition RAM	1,5	1

MNEMONIC	DEFINITION	SCHEMATICS	ORIGIN
XE/TRIG	Trigger signal from glitch chip. May be either HIGH or LOW true, depending on XE/TRIGPOL.	4,5	4
XE/TRIGPOL	Trigger polarity. Determines whether trigger will be HIGH or LOW true for an AND/OR combination with a trigger from another acquisition board.	4,5	4
HE/TSTENCK	Test enable memory address counter clock.	1,2	1
LE/WRT	Write. Enables write to acquisition RAM.	1,2	1
LE/WRTX	Write enable from U22 encoder to X memory bank.	2,4	4
LE/WRTY	Write enable from U22 encoder to Y memory bank.	2,4	4
H/XADR0-7	Address lines from the encoders to the X memory bank.	2,5	2
H/YADR0-7	Address lines from the encoders to the Y memory bank.	2,5	2
H/XCH0D0-7 * H/XCH1D0-7 * H/XCH2D0-7 * H/XCH3D0-7 * H/XCH4D0-7 * H/XCH5D0-7 * H/XCH6D0-7 * H/XCH7D0-7 *	X channel data. Encoder output from each probe channel to X memory bank.	4,5	4
H/YCH0D0-7 * H/YCH1D0-7 * H/YCH2D0-7 * H/YCH3D0-7 * H/YCH4D0-7 * H/YCH5D0-7 * H/YCH6D0-7 * H/YCH7D0-7 *	Y channel data. Encoder output from each probe channel to Y memory bank.	4,5	4

Table 8-2. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

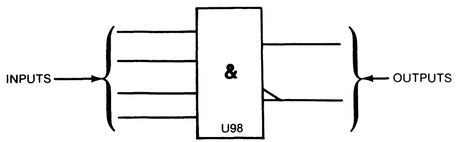
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

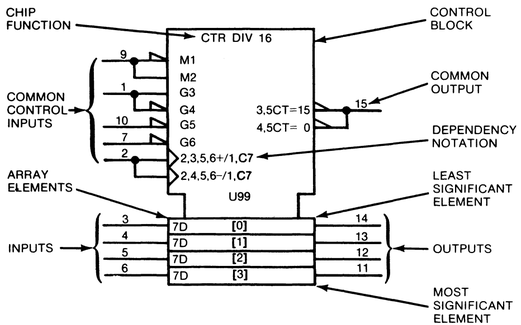
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

LS-08-09-82 - 1

Table 8-2. Logic Symbols (Cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-2. Logic Symbols (Cont'd)

OTHER SYMBOLS

Analog Signal	Inversion	Shift Right (or down)
& AND	O Negation	/ Solidus (allows an input or output to have more than one function)
Bit Grouping	Nonlogic Input/Output	
Buffer	Open Circuit (external resistor)	▽ Tri-State
! Compare	Open Circuit (external resistor)	, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
Dynamic	≥1 OR	
=1 Exclusive OR	Passive Pull Down (internal resistor)	( ) Used for factoring terms using algebraic techniques.
Hysteresis	Passive Pull Up (internal resistor)	[ ] Information not defined.
? Interrogation	Postponed	Φ Logic symbol not defined due to complexity.
Internal Connection	← Shift Left (or up)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	–	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

Astable

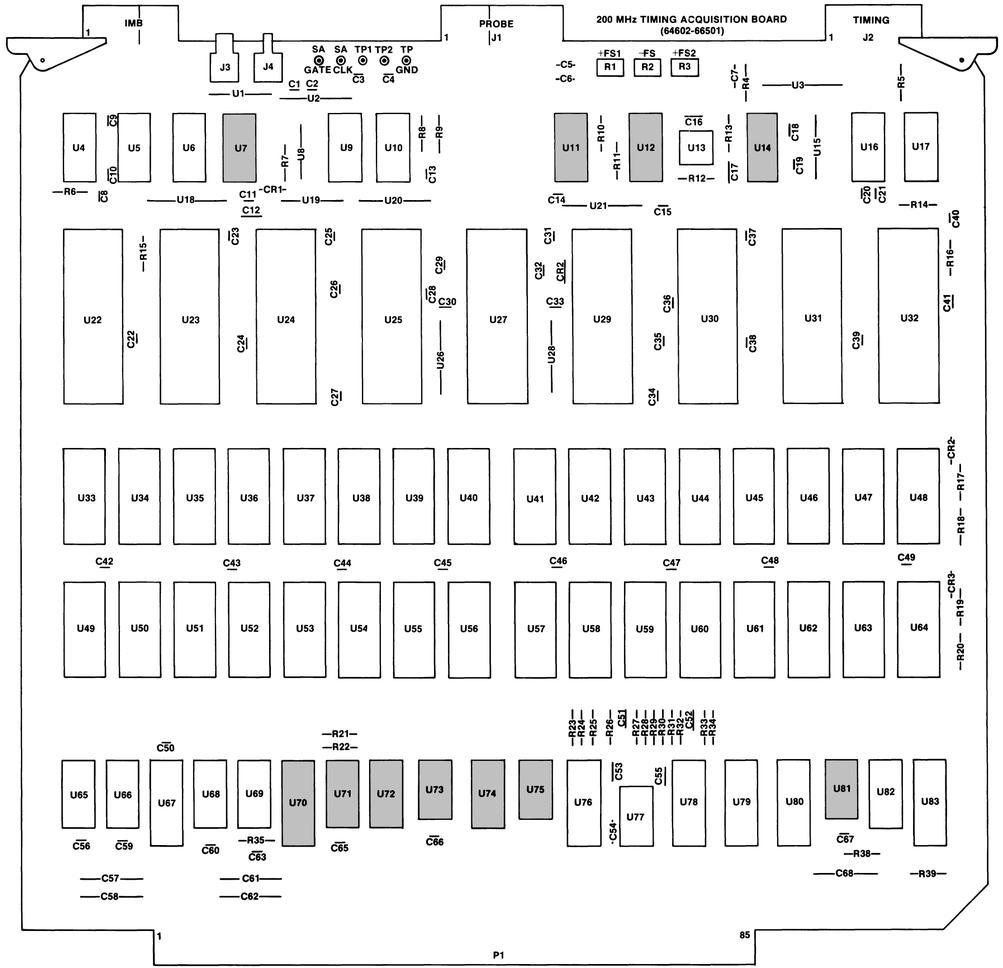
100 ns Delay

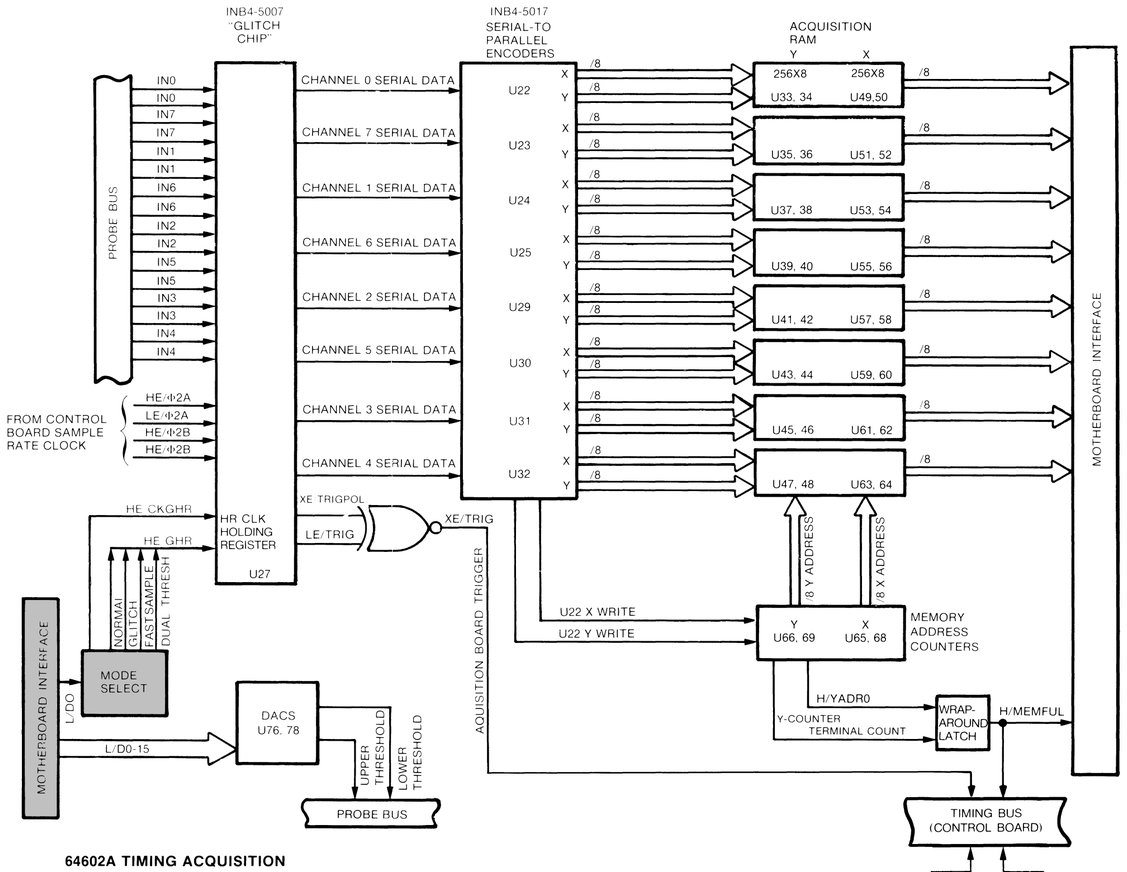
Nonretriggerable Monostable

NV Nonvolatile

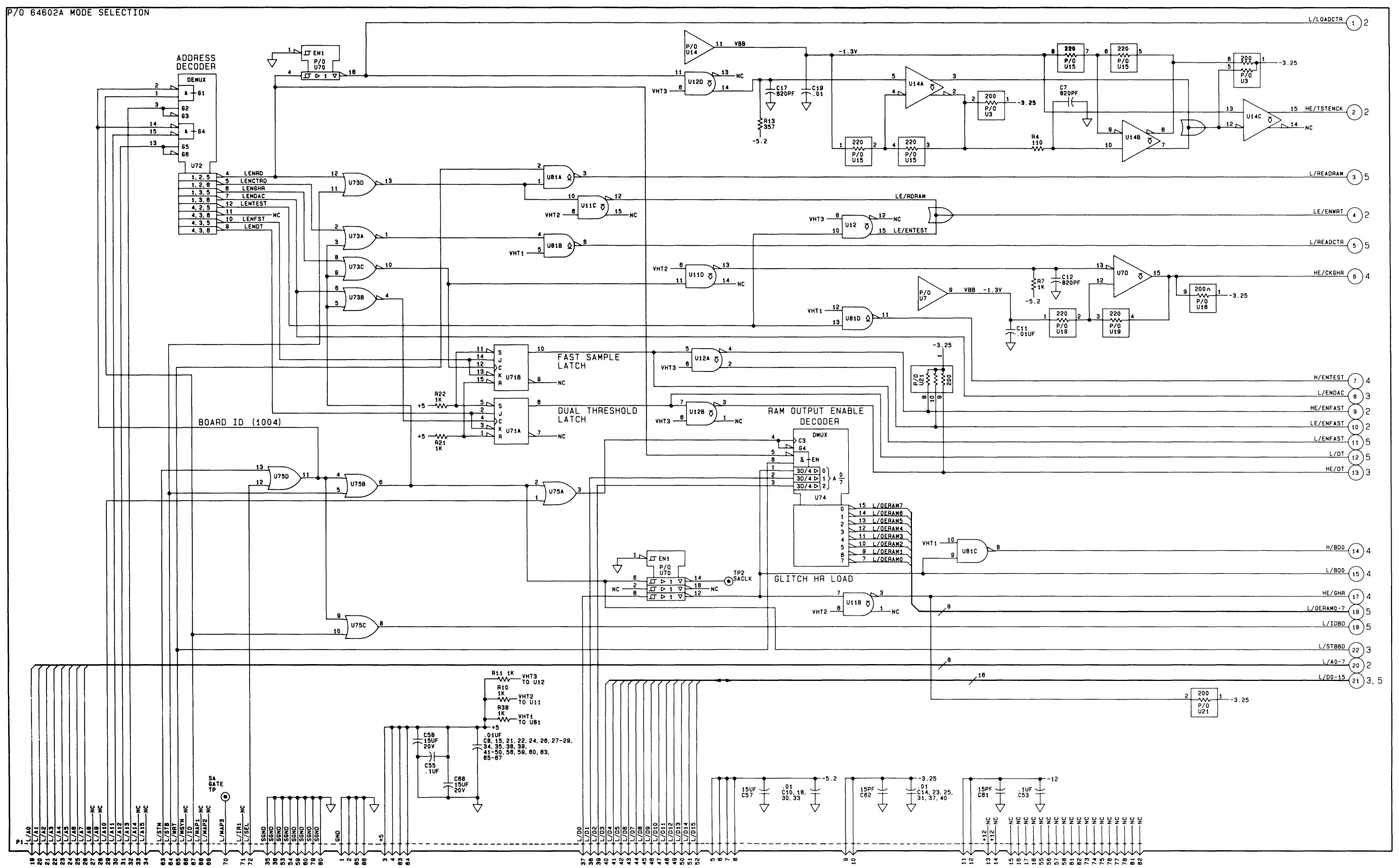
Retriggerable Monostable

LS-08-09-82 - 3





64602A TIMING ACQUISITION BOARD



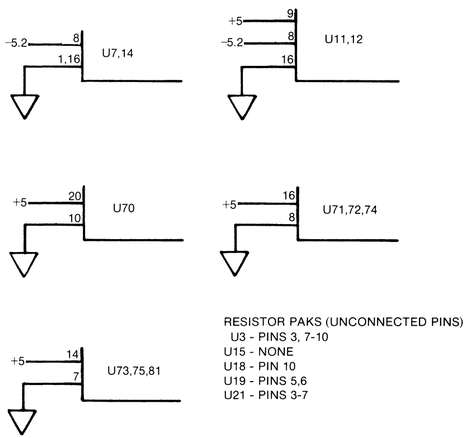
ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr. Part No.
U7	1820-0920	MC1692L
U11,12	1820-1173	MC10124L
U14	1820-0810	MC10116P
U70	1820-2024	SN74LS244N
U71	1820-1282	SN74LS109
U72	1820-1245	SN74LS155N
U73	1820-1144	SN74LS02N
U74	1820-2550	SN74LS137N
U75	1820-2657	SN74ALS32N
U81	1820-2646	SN74ALS00N

PARTS ON THIS SCHEMATIC

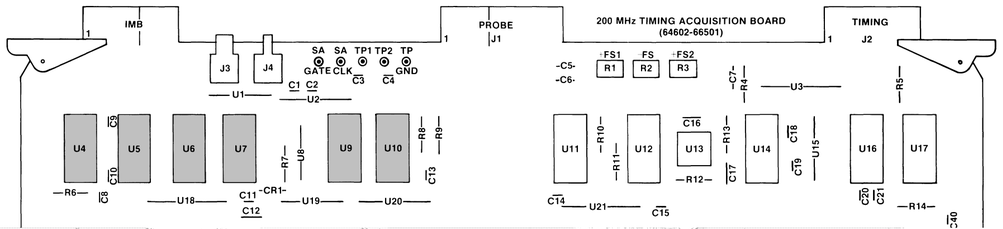
C7,8,10-12,14,15,17-19,21-31,33-50,53,55-68
R4,7,10,11,13,21,22,38
TP (SA GATE)
U3,15,18,19,21 (resistor packs)

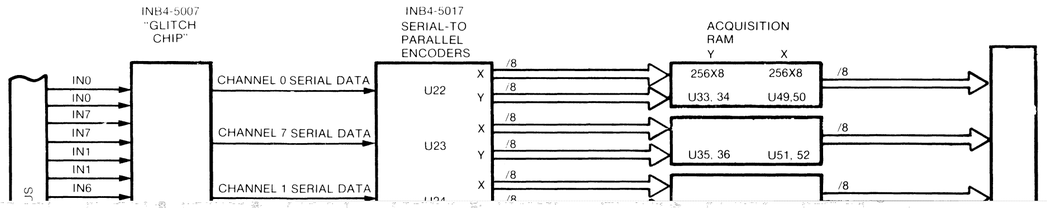
IC POWER SUPPLY CONFIGURATION

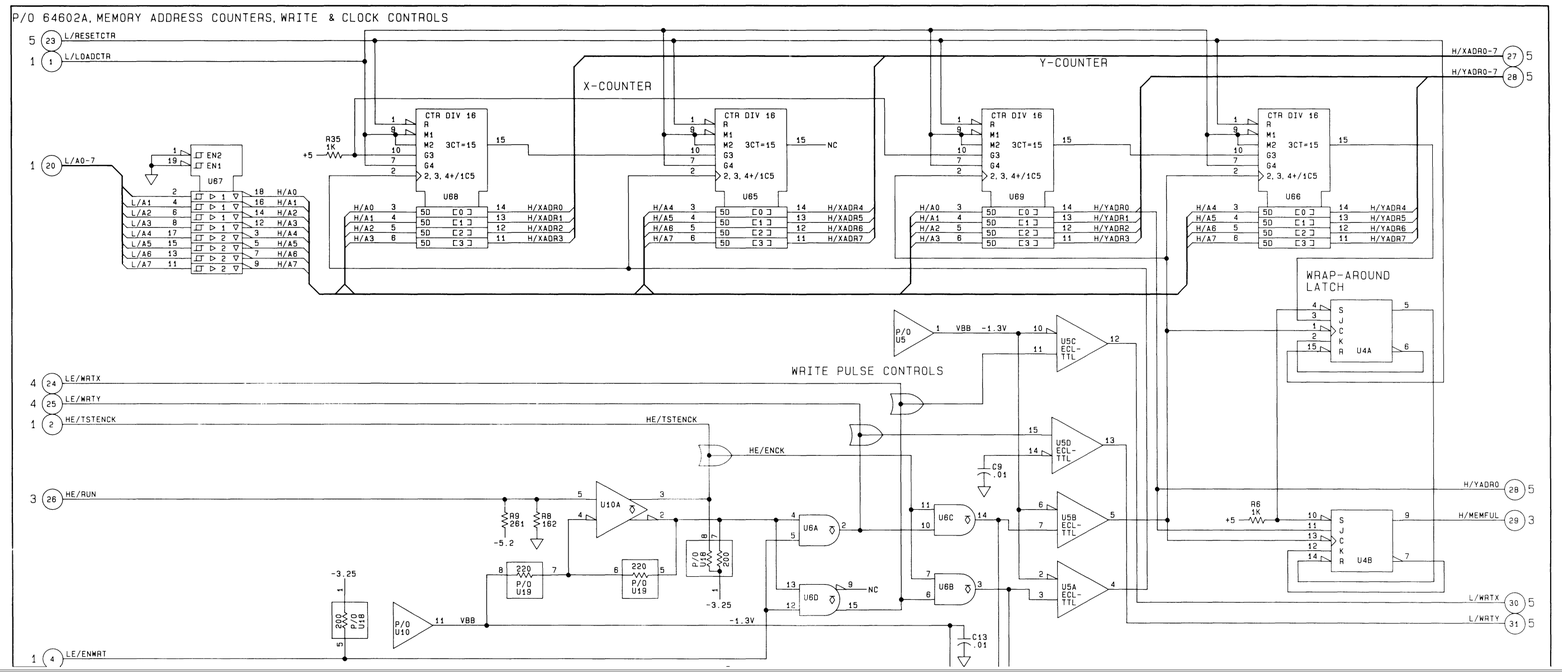


RESISTOR PAKS (UNCONNECTED PINS)
U3 - PINS 3, 7-10
U15 - NONE
U18 - PIN 10
U19 - PINS 5,6
U21 - PINS 3-7

Figure 8-5.
Service Sheet 1
Mode Selection
ACQ 8-15


IMB
PROBE
J1
200 MHz TIMING ACQUISITION BOARD
(64602-66501)
TIMING
J2
J3
J4
SA GATECLK
SA
TP1
TP2
TP
GND
-FS1
FS
+FS2
R1
R2
R3
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
CR1


INB4-5007
"GLITCH
CHIP"
INB4-5017
SERIAL-TO
PARALLEL
ENCODERS
ACQUISITION
RAM
Y
X
IN0
IN0
IN7
IN7
IN1
IN1
IN6
CHANNEL 0 SERIAL DATA
CHANNEL 7 SERIAL DATA
CHANNEL 1 SERIAL DATA
U22
U23
/8
256X8
U33, 34
U49,50
U35, 36
U51, 52



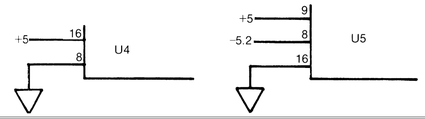
ICs ON THIS SCHEMATIC

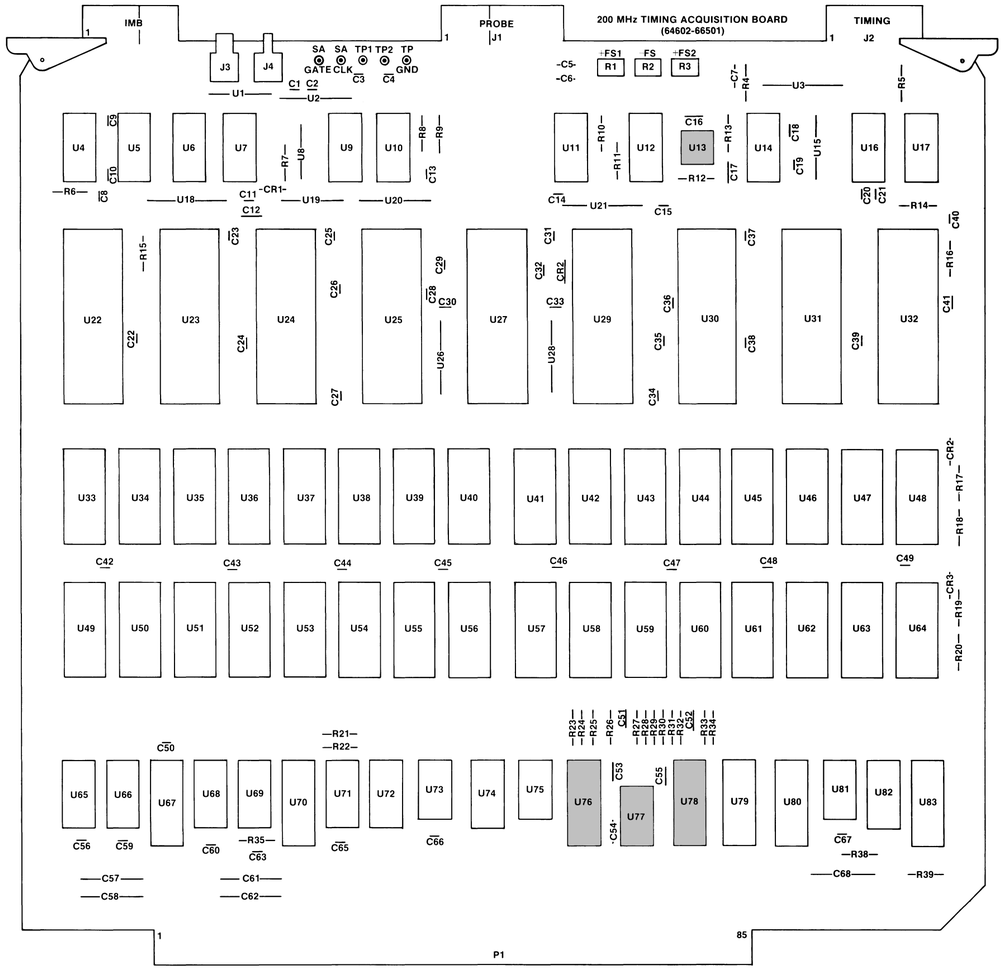
Ref Des	HP Part No.	Mfr. Part No.
U4	1820-1212	SN74LS112AN
U5	1820-1052	MC10125L
U6	1820-1400	MC10104P
U7	1820-0920	MC1692L
U9	1820-0796	MC1662L
U10	1820-1320	MC10216L
U65,66,68,69	1820-2890	93S16DC
U67	1820-1917	SN74LS240N

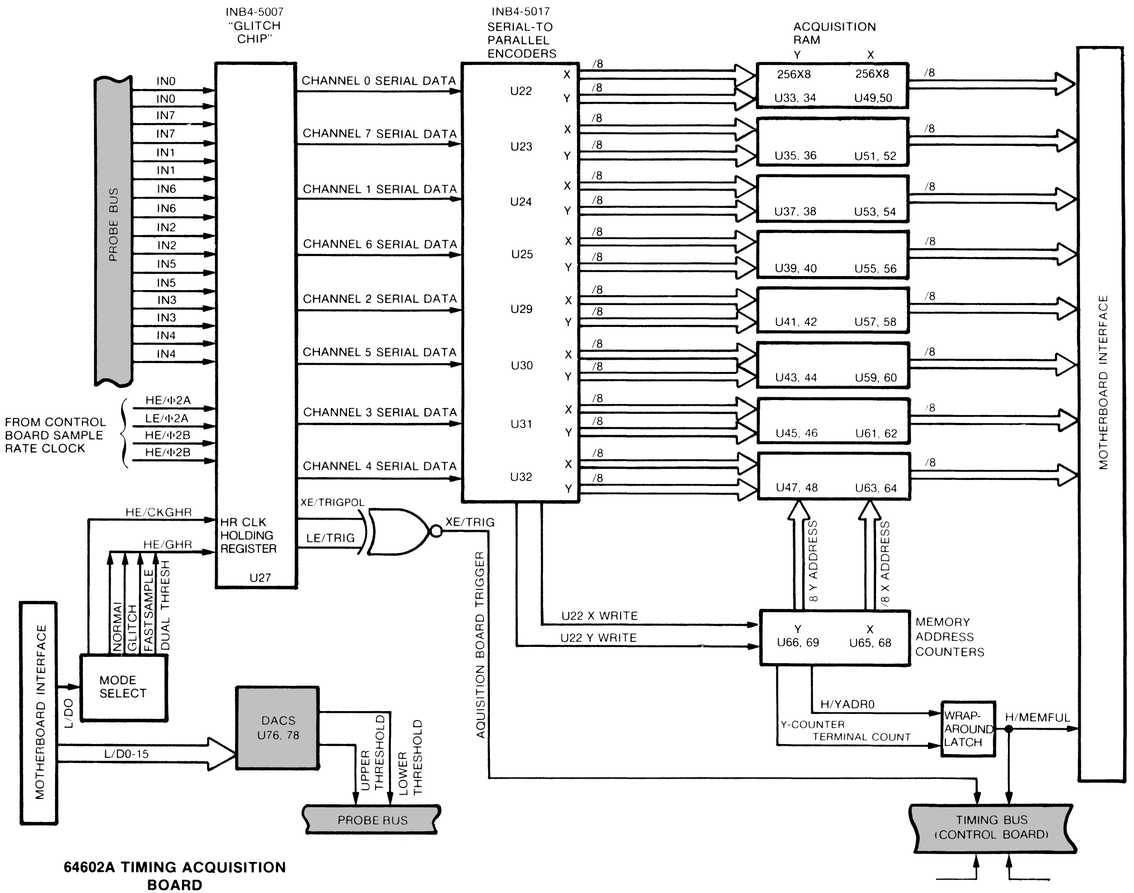
PARTS ON THIS SCHEMATIC

C1,2,9,13,
CR1
R6,8,9,35
U1,2,8,18,19,20 (resistor packs)

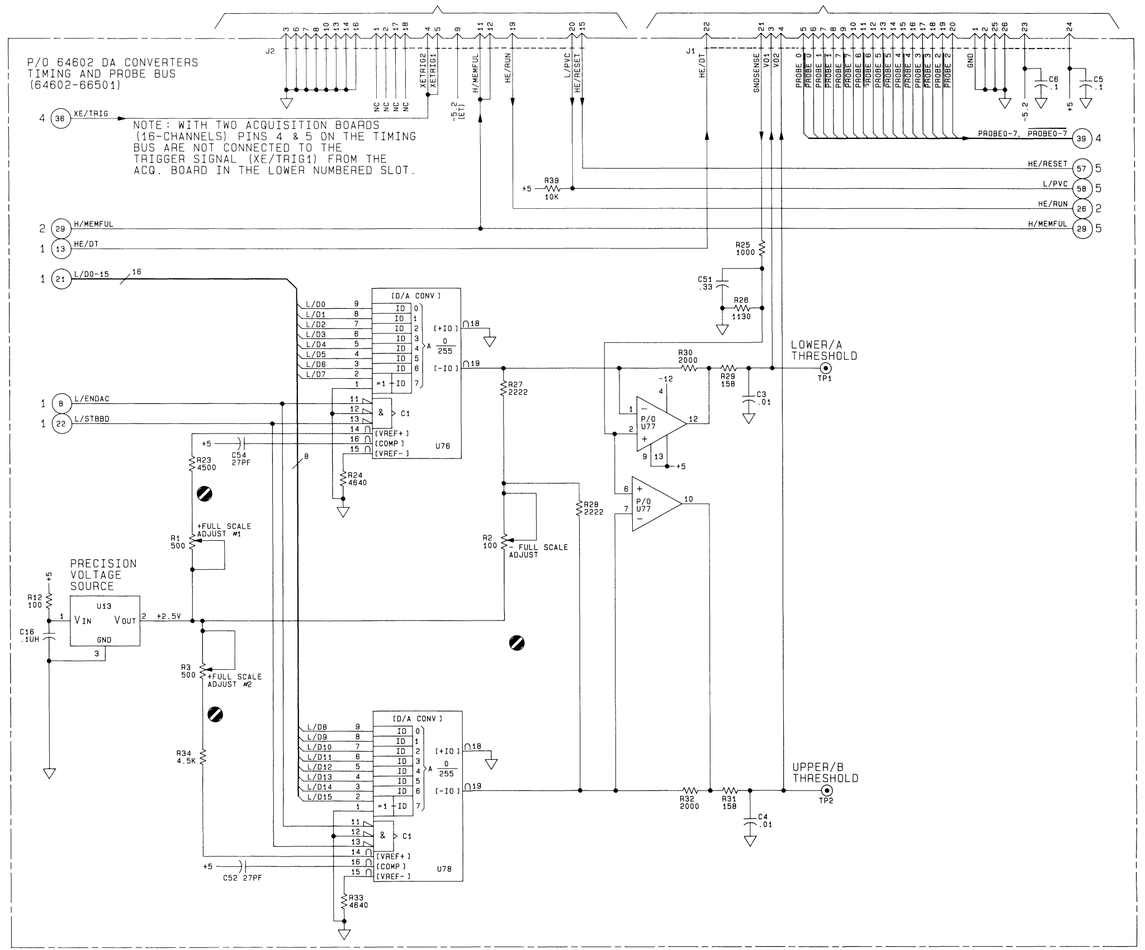
IC POWER SUPPLY CONFIGURATION







64602A TIMING ACQUISITION BOARD



ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr. Part No.
U13	1826-0544	1403U
U76,78	1826-0856	6080A
U77	1826-0974	747

PARTS ON THIS SCHEMATIC

C3-6,16,51,52,54
R1-3,23-34
TP1,2

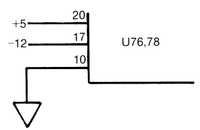
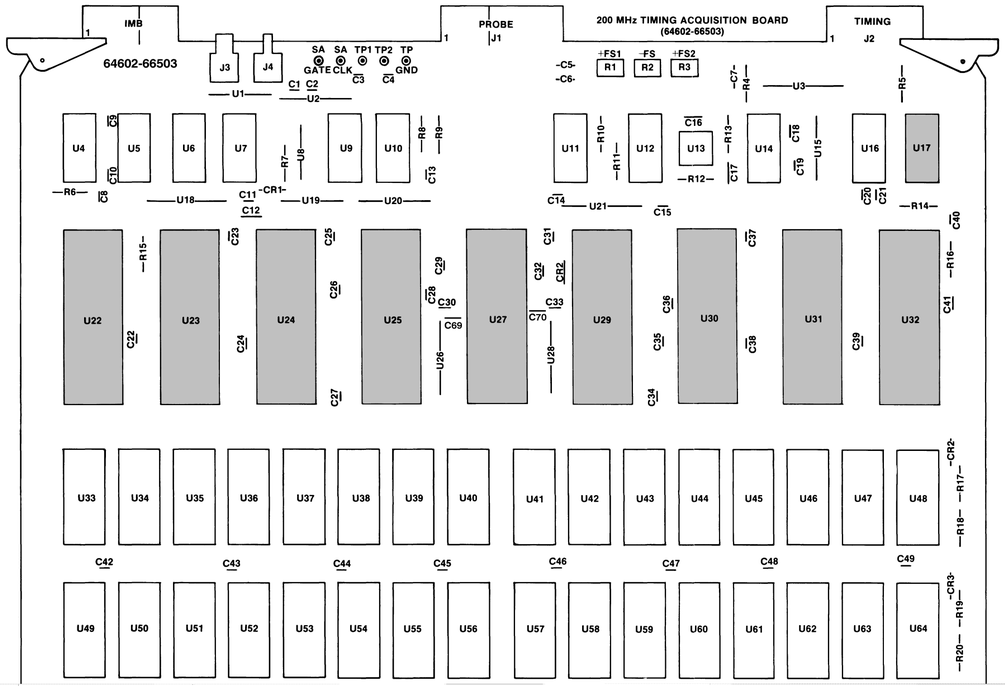
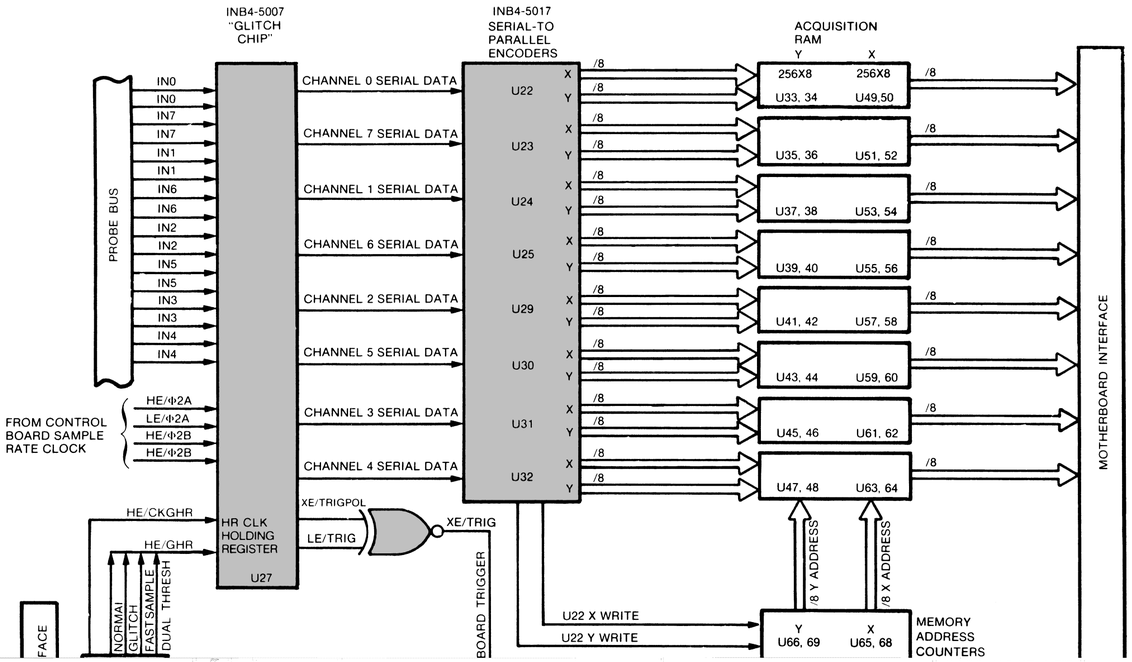
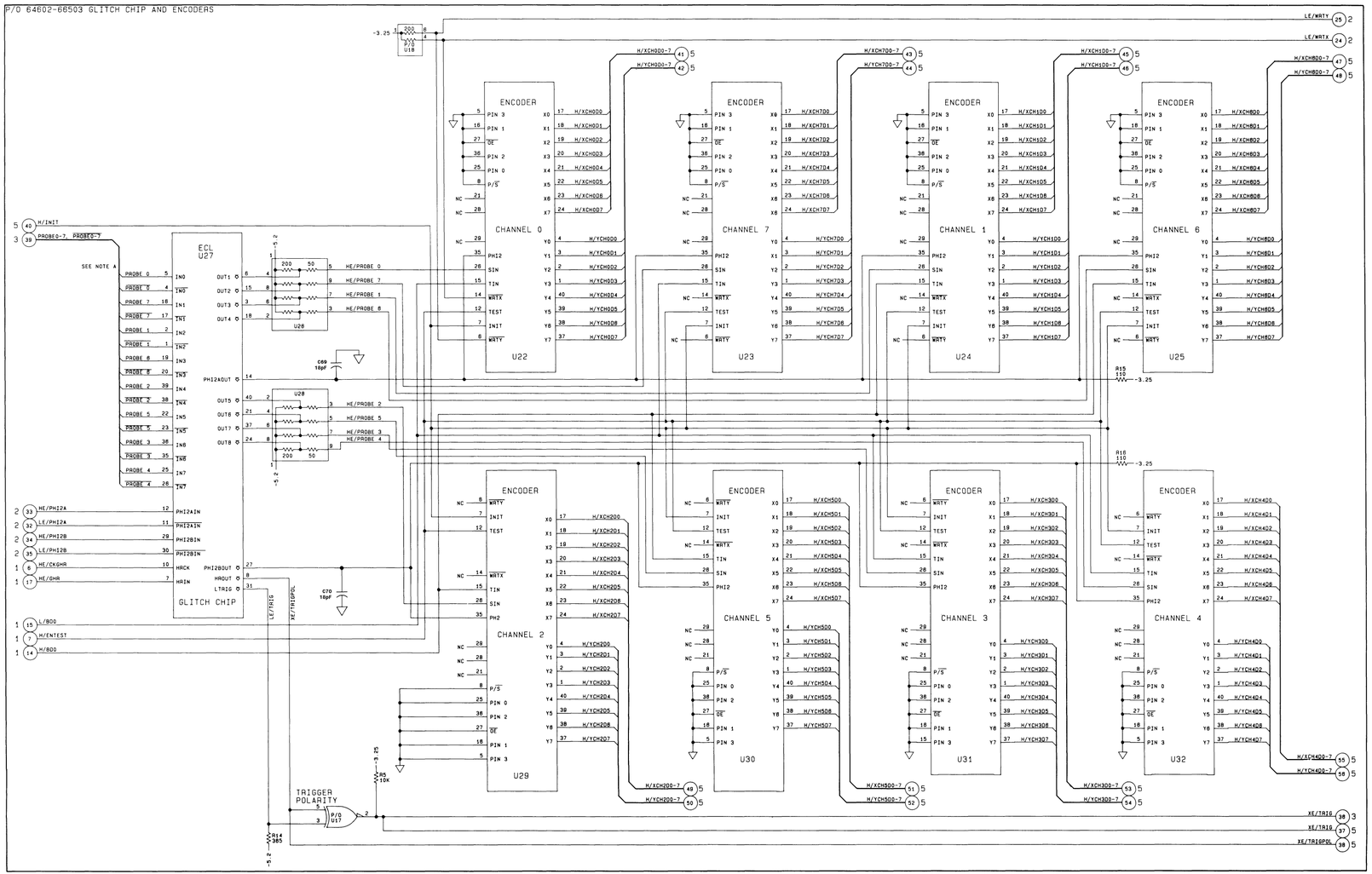


Figure 8-7.
Service Sheet 3
DACs, Probe Bus, & Timing Bus
Change 1


IMB
64602-66503
J3
J4
SA GATE
SA CLK
TP1
TP2
TP GND
PROBE
J1
200 MHz TIMING ACQUISITION BOARD (64602-66503)
TIMING
J2
+FS1
+FS
+FS2
R1
R2
R3
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U27
U29
U30
U31
U32
U33
U34
U35
U36
U37
U38
U39
U40
U41
U42
U43
U44
U45
U46
U47
U48
U49
U50
U51
U52
U53
U54
U55
U56
U57
U58
U59
U60
U61
U62
U63
U64


INB4-5007 "GLITCH CHIP"
INB4-5017 SERIAL-TO PARALLEL ENCODERS
ACQUISITION RAM
Y
X
256X8
U33, 34
U49,50
U35, 36
U51, 52
U37, 38
U53, 54
U39, 40
U55, 56
U41, 42
U57, 58
U43, 44
U59, 60
U45, 46
U61, 62
U47, 48
U63, 64
PROBE BUS
IN0
IN7
IN1
IN6
IN2
IN5
IN3
IN4
CHANNEL 0 SERIAL DATA
CHANNEL 7 SERIAL DATA
CHANNEL 1 SERIAL DATA
CHANNEL 6 SERIAL DATA
CHANNEL 2 SERIAL DATA
CHANNEL 5 SERIAL DATA
CHANNEL 3 SERIAL DATA
CHANNEL 4 SERIAL DATA
FROM CONTROL BOARD SAMPLE RATE CLOCK
HE/Φ2A
LE/Φ2A
HE/Φ2B
LE/Φ2B
HE/CKGHR
HE/GHR
HR CLK HOLDING REGISTER
U27
XE/TRIGPOL
LE/TRIG
XE/TRIG
BOARD TRIGGER
NORMAL
GLITCH
FAST SAMPLE
DUAL THRESH
/8
/8 Y ADDRESS
/8 X ADDRESS
U22 X WRITE
U22 Y WRITE
Y
U66, 69
X
U65, 68
MEMORY ADDRESS COUNTERS
MOTHERBOARD INTERFACE



ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr. Part No.
U17	1820-0793	MC1674L
U22-25,29-32	1NB4-5017	
U27	1NB4-5007	

PARTS ON THIS SCHEMATIC

C69
C70
C4
CR2
R5
Q1
U26,28 (resistor packs)

IC POWER SUPPLY CONFIGURATION

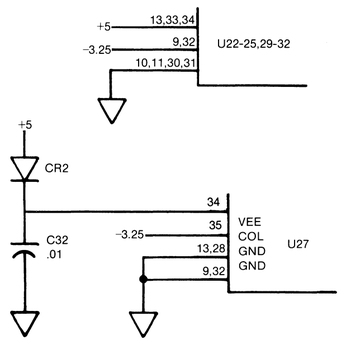
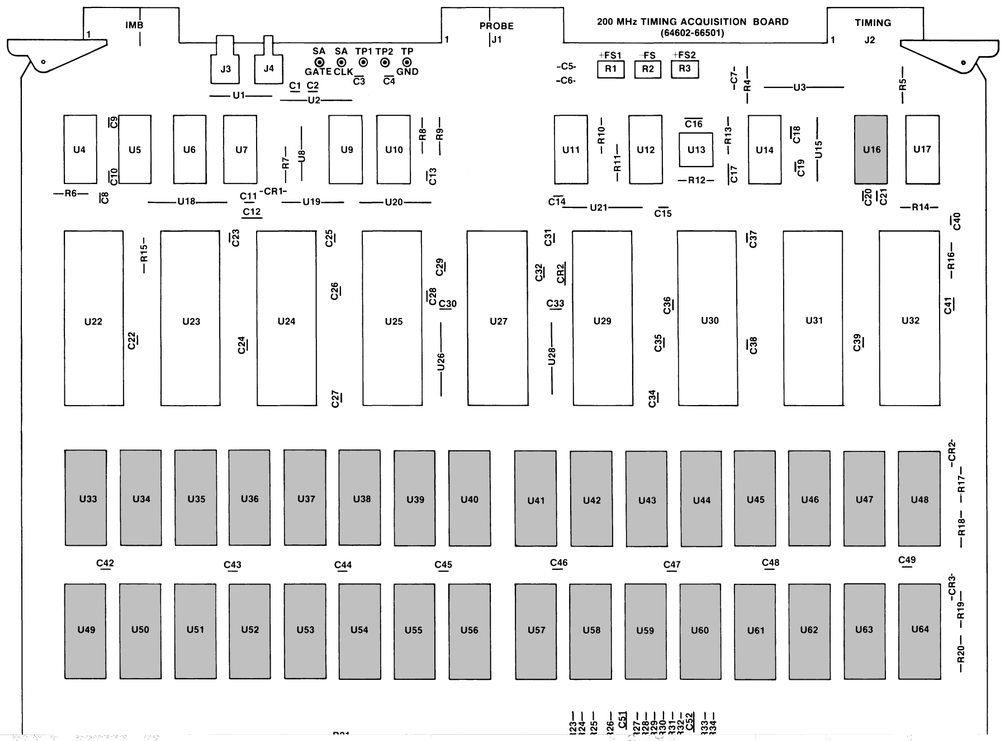
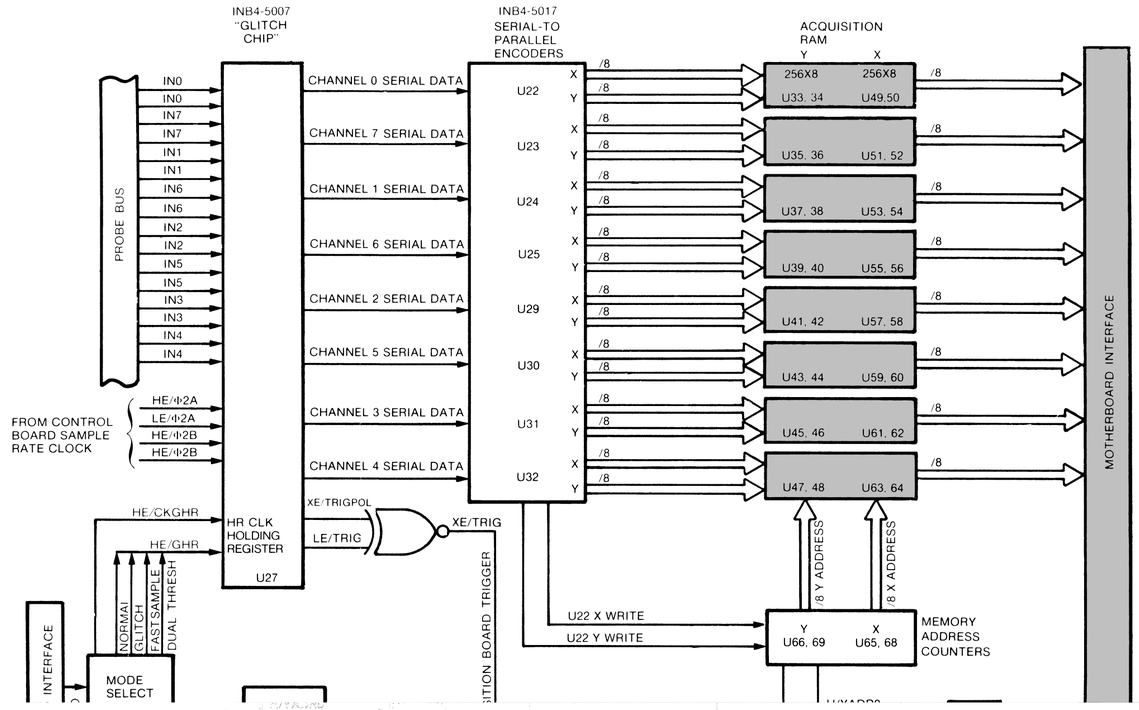


Figure 8-8.
Service Sheet 4
Glitch Chip & Encoders
Change 1 ACQ 8-21


IMB
PROBE
J1
200 MHz TIMING ACQUISITION BOARD
(64602-66501)
TIMING
J2
J3
J4
SA GATE
SA CLK
TP1
TP2
TP GND
+FS1
-FS
+FS2
R1
R2
R3
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U27
U29
U30
U31
U32
U33
U34
U35
U36
U37
U38
U39
U40
U41
U42
U43
U44
U45
U46
U47
U48
U49
U50
U51
U52
U53
U54
U55
U56
U57
U58
U59
U60
U61
U62
U63
U64

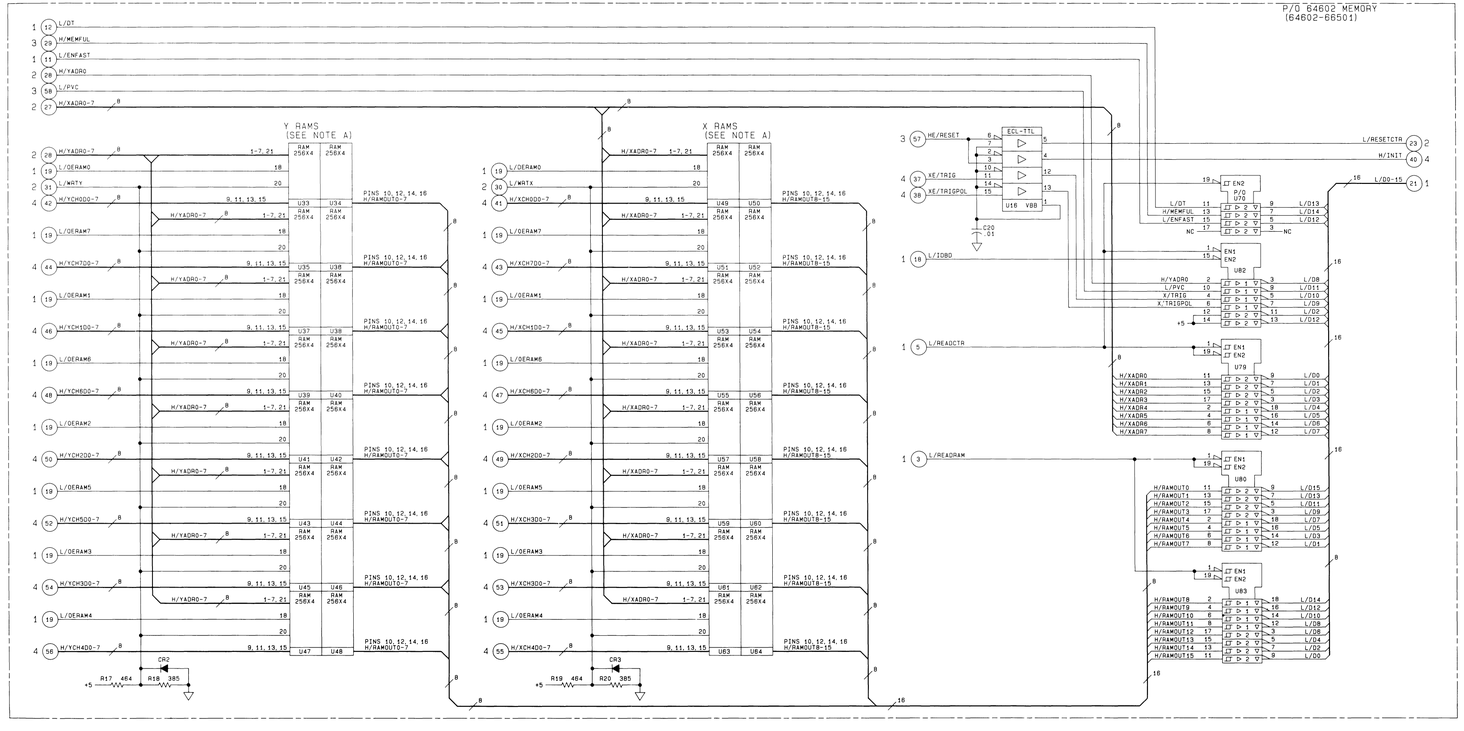

INB4-5007
"GLITCH
CHIP"
INB4-5017
SERIAL-TO
PARALLEL
ENCODERS
ACQUISITION
RAM
Y
X
256X8
U33, 34
U49,50
U35, 36
U51, 52
U37, 38
U53, 54
U39, 40
U55, 56
U41, 42
U57, 58
U43, 44
U59, 60
U45, 46
U61, 62
U47, 48
U63, 64
MOTHERBOARD INTERFACE
PROBE BUS
IN0
IN7
IN1
IN6
IN2
IN5
IN3
IN4
CHANNEL 0 SERIAL DATA
CHANNEL 7 SERIAL DATA
CHANNEL 1 SERIAL DATA
CHANNEL 6 SERIAL DATA
CHANNEL 2 SERIAL DATA
CHANNEL 5 SERIAL DATA
CHANNEL 3 SERIAL DATA
CHANNEL 4 SERIAL DATA
U22
U23
U24
U25
U29
U30
U31
U32
/8
FROM CONTROL
BOARD SAMPLE
RATE CLOCK
HE/Φ2A
LE/Φ2A
HE/Φ2B
HE/Φ2B
HE/CKGHR
HE/GHR
HR CLK
HOLDING
REGISTER
U27
XE/TRIGPOL
LE/TRIG
XE/TRIG
NORMAL
GLITCH
FAST SAMPLE
DUAL THRESH
MODE
SELECT
/8 Y ADDRESS
/8 X ADDRESS
U22 X WRITE
U22 Y WRITE
Y
U66, 69
X
U65, 68
MEMORY
ADDRESS
COUNTERS

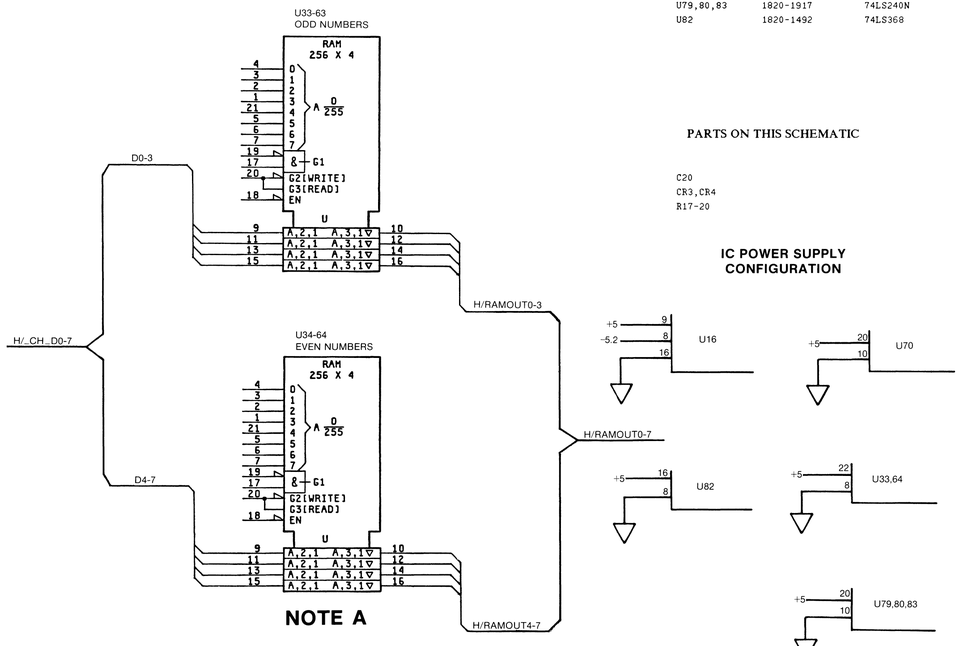
ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr. Part No.
U16	1820-1052	MC10125L
U33-64	1816-1476	93L422DC SLT
U70	1820-2024	74LS244N
U79,80,83	1820-1917	74LS240N
U82	1820-1492	74LS368

PARTS ON THIS SCHEMATIC

C20
CR3,CR4
R17-20





IC POWER SUPPLY CONFIGURATION

Figure 8-9.
Service Sheet 5
Acquisition Memory
ACQ 8-23

SALES & SUPPORT OFFICES

Arranged alphabetically by country

Product Line Sales/Support Key

Key	Product Line
A	Analytical
CM	Components
C	Computer Systems Sales only
CH	Computer Systems Hardware Sales and Services
CS	Computer Systems Software Sales and Services
E	Electronic Instruments & Measurement Systems
M	Medical Products
MP	Medical Products Primary SRO
MS	Medical Products Secondary SRO
P	Personal Computation Products
*	Sales only for specific product line
**	Support only for specific product line

IMPORTANT: These symbols designate general product line capability. They do not insure sales or support availability for all products within a line, at all locations. Contact your local sales office for information regarding locations where HP support is available for specific products.

HP distributors are printed in italics.

ANGOLA

Telectra
Empresa Técnica de Equipamentos
R. Barbosa Rodrigues, 41-I DT.
Caixa Postal 6487
LUANDA
Tel: 35515,35516
E,M,P

ARGENTINA

Hewlett-Packard Argentina S.A.
Avenida Santa Fe 2035
Martinez 1640 **BUENOS AIRES**
Tel: 798-5735, 792-1293
Telex: 17595 BIONAR
Cable: HEWPACKARG
A,E,CH,CS,P

Biotron S.A.C.I.M. e I.
Av Paseo Colon 221, Piso 9
*1399 **BUENOS AIRES***
Tel: 30-4846, 30-1851
Telex: 17595 BIONAR
M

AUSTRALIA

Adelaide, South Australia Office

Hewlett-Packard Australia Ltd.
153 Greenhill Road
PARKSIDE, S.A. 5063
Tel: 272-5911
Telex: 82536
Cable: HEWPARD Adelaide
A*,CH,CM,,E,MS,P

Brisbane, Queensland Office

Hewlett-Packard Australia Ltd.
10 Payne Road
THE GAP, Queensland 4061
Tel: 30-4133
Telex: 42133
Cable: HEWPARD Brisbane
A,CH,CM,E,M,P

Canberra, Australia Capital Territory Office

Hewlett-Packard Australia Ltd.
121 Wollongong Street
FYSHWICK, A.C.T. 2609
Tel: 80 4244
Telex: 62650
Cable: HEWPARD Canberra
CH,CM,E,P

Melbourne, Victoria Office

Hewlett-Packard Australia Ltd.
31-41 Joseph Street
BLACKBURN, Victoria 3130
Tel: 890 6351
Telex: 31-024
Cable: HEWPARD Melbourne
A,CH,CM,CS,E,MS,P

Perth, Western Australia Office

Hewlett-Packard Australia Ltd.
261 Stirling Highway
CLAREMONT, W.A. 6010
Tel: 383-2188
Telex: 93859
Cable: HEWPARD Perth
A,CH,CM,,E,MS,P

Sydney, New South Wales Office

Hewlett-Packard Australia Ltd.
17-23 Talavera Road
P.O. Box 308
NORTH RYDE, N.S.W. 2113
Tel: 887-1611
Telex: 21561
Cable: HEWPARD Sydney
A,CH,CM,CS,E,MS,P

AUSTRIA

Hewlett-Packard Ges.m.b.h.
Grottenhofstrasse 94
Verkaufsburo Graz
A-8052 **GRAZ**
Tel: 291-5-66
Telex: 32375
CH,E*

Hewlett-Packard Ges.m.b.h.
Lieblgasse 1
P.O. Box 72
A-1222 **VIENNA**
Tel: (0222) 23-65-11-0
Telex: 134425 HEPA A
A,CH,CM,CS,E,MS,P

BAHRAIN

Green Salon
P.O. Box 557
BAHRAIN
Tel: 255503-255950
Telex: 84419
P

Wael Pharmacy
P.O. Box 648
BAHRAIN
Tel: 256123
Telex: 8550 WAEL BN
E,M

BELGIUM

Hewlett-Packard Belgium S.A./N.V.
Blvd de la Woluwe, 100
Woluwedal
B-1200 **BRUSSELS**
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BRAZIL

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Hewlett-Packard do Brasil I.e.C. Ltda.
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***BOMBAY** 400 025*
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***SECUNDERABAD** 500 003*
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P.O.Box 1917
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*Kuching, **SARAWAK***
Tel: 36299
Telex: MA 70904 PROTEL
Cable: PROTELENG
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MALTA

Philip Toledo Ltd.
Notabile Rd.
MRIEHEL
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Telex: Media MW 649
P

MEXICO

Hewlett-Packard Mexicana, S.A.
de C.V.
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MEXICO D.F. 16020
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Telex: 17-74-507 HEWPACK MEX
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Hewlett-Packard Mexicana, S.A.
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Col. del Valle
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CH

ECISA
José Vasconcelos No. 218
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***MEXICO** D.F. 06140*
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M

MOROCCO

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CASABLANCA
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E

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CASABLANCA
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P

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NL1180 AR **AMSTELVEEN**
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NL 2900AA **CAPELLE, A/D IJSSEL**
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AUCKLAND
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110 Mandeville St.
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A,M

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OMAN

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P

Suhail & Saud Bahwan
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Telex: 3274 BAHWAN MB

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Cable: FEMUS Rawalpindi
A,E,M

Mushko & Company Ltd.
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Telex: 2894 MUSKO PK
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Electrónico Balboa, S.A.
Calle Samuel Lewis, Ed. Alfa
Apartado 4929
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CM,E,M,P

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P.O. Box 2649 Manila
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Telex: 40018, 42000 ITT GLOBE MACKAY BOOTH
P

PORTUGAL

Mundinter
Intercambio Mundial de Comércio S.A.R.L.
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M

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P

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Telex: 4806 CHPARB
P

Eastern Technical Services
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Nasser Trading & Contracting
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M

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Middle East Electronics
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M,P

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A

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Unimesa
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Telex: 84439 Simonco TH
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Corema
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M

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Teknim Company Ltd.
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*Kavaklidere, **ANKARA***
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E

E.M.A.
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M

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March 1983 5952-6900

HP distributors are printed in italics.

64602-90902, NOVEMBER 1982
Replaces: 64602-90901, October 1982

PRINTED IN U.S.A.